QYH500 Family

LPGA

Design

Manual

Laser-Programmable
Gate Arrays

Chip Express Corporation

Chip Express®

The ASIC Time-to-Market Solution™

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Laser-Programmable Gate Arrays
QYH500 Family

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1.1 Introduction to Chip Express

Technology

Chip Express uses a unique, patented approach in developing gate arrays that give it the ability to customize chips rapidly. Our LPGA technology uses a disconnect methodology which starts with a fully fabricated, double-metal, CMOS gate array that has all possible metal interconnections already made. Chip Express then removes, in a single step, the metal that is not needed, by using pulses of laser light, that have a tolerance in the range of 0.1μ. Our OneMask technology allows us to translate your LPGA prototype into medium-volume production, by using a single metal-etch step.

Signal Interface

The number of bi-directional I/O pads range from 76 to over 400. All I/Os are both latch-up and electrostatic-discharge protected. Input macros which provide CMOS input thresholds, TTL thresholds, internal pull-ups, internal pull-downs, and w/wo hysteresis can be selected. Output macros can be selected that are tri-state, totem-pole, or open N and open P drains, with or without slew-rate control, and which can provide active drive of 2mA, 4mA, 8mA, 12mA or 16mA.

Product Options

Chip Express uses one of three methods to customize the part for the customer, depending on the quantity of devices needed. All three methods use the same relative placement, and have the same functionality and performance.

The customer's netlist is transformed into a physical layout of the chip, using Chip Express proprietary software. This layout, which is the same as conventional gate array layouts, is used to drive one of three methods of customization:

	Type of Run	Quantity	Process	Time
Option 1	Prototype	Small	LPGA	1-5 days
Option 2	Pre-Production	Medium*	OneMask®	1-3 weeks
Option 3	Volume Production	Large*	HARD Array™	5-6 weeks

* Economic volumes will depend upon technology family and die size.

Option 1. LPGA

For ***prototyping***, Chip Express uses a proprietary laser-based system, the QuICk® System, to disconnect the metal layers. The laser disconnect process is automatic, driven by a "cut-list" that was generated from the Chip Express layout software. Processing one die at a time, the laser makes up to 10,000 cuts per second, with millions of cuts made per chip. The result of this process is a fully functional gate array in just a few hours.

Chip Express' standard prototype turn-around time is five days from approved netlist. Shorter turn-around times, such as one day, are available. Chip Express has a "no-sign-off" policy on prototypes, whereby only a phone call from the customer is required for the design netlist to be released to silicon. The standard prototype set is two parts, packaged and tested per the customer's requirements. Additional prototype parts can be obtained by the customer if needed.

1.1 Introduction to Chip Express (con't.)

Option 2. OneMask®

For *pre-production* or low volume requirements, Chip Express offers its *OneMask*® process. The same layout is used and converted into mask data by the Chip Express layout software. A single mask etches away the unneeded metal in both layers (instead of the laser cutting used in prototyping). Processing is done by conventional photolithography, at the wafer level. This process results in throughput times of 1 to 2 weeks.

The pre-production volume option is typically used by customers for engineering samples, beta sites, etc., when dozens to hundreds of parts are required quickly. For the pre-production *OneMask*® option, devices are shipped to the customer in 1-3 weeks.

The *OneMask*® Gate Array provides an ideal transition, or "bridge", from the fast-turnaround LPGA prototypes to the higher volume production of the *HARD* Array™.

Option 3. HARD Array

Volume production typically has a 6 week lead time. Chip Express' *HARD Array*™ (High Area Reduction Die) technology provides low cost, small die size production units equivalent in performance to laser-programmable fast-turn prototype parts. "Compacting" is performed by proprietary Chip Express software that maps the LPGA prototype into a denser silicon array without altering the relative placement or routing of the logic cells. The same number of logic columns and rows are used, and the relative length of all the nets are preserved.

The reduced length of the metal nets is compensated for by a reduction of the transistor's widths, and by modification of the metal line width. If production is supplied by a different vendor, the routing is not preserved. Only Chip Express preserves placement and routing so that the P&R software may maintain equivalent path delays.

A design which is intended for high volume production will be completed by the customer using popular schematic programs, and the QYH500 LPGA design libraries which support Synopsys, Cadence, Viewlogic, and Mentor. Once the LPGA prototypes are approved by the customer, the design is compacted by Chip Express onto a corresponding-density HARD Array.

To verify production readiness of the design, two laser-cut parts will be provided that represent the best and worst case (fastest and slowest) corners of the production process. All production units will fall within the extremes of the two prototype devices. Following customer approval, a pre-production run will be fabricated on a lot of the *HARD Array*™ wafers, and shipped in the final production package. After pre-production device approval from the customer, full volume production deliveries begin.

1.2 Introduction to CAE Tools

The designer should select the tools that he or she is familiar with. QuICk® software from Chip Express supports the following popular CAE tools;

	Schematic	Simulation	Synthesis	Static Timing
Verilog-XL		Sun, HP		
Synopsys		VSS* - Sun, HP	Sun, HP	Sun, HP
ViewLogic	PC, Sun	PC, Sun		
Mentor 8.0*	Sun, HP	Sun, HP		
Motive*				Sun, HP

* Preliminary and libraries undergoing certification

Release versions are not shown above, because they are frequently updated. Please check with Chip Express for the most recent version.

Each design kit contains a software manual, release notes, magnetic media containing the software, and the selected QYHx00 family macrocell library plus databook. Refer to page 83 for complete design kit descriptions.

Netlist Support

Chip Express supports the Verilog, EDIF and DDF netlist formats. Chip Express also accepts netlist input in the following formats :

Actel - ADL	Synopsys - DB	VLSI - NLS
Mentor - mifflist	TI - HDL	Xilinx - XNF

Test Vector Support

Chip Express prefers the standard CTV (Chip Express Test Vector) format. Chip Express also accepts test vector input in the following formats :

TI - TDL		YTV - (Chip Express print on change)
TSSI	WIF(Vss)	VLSI - (tabular trace file)

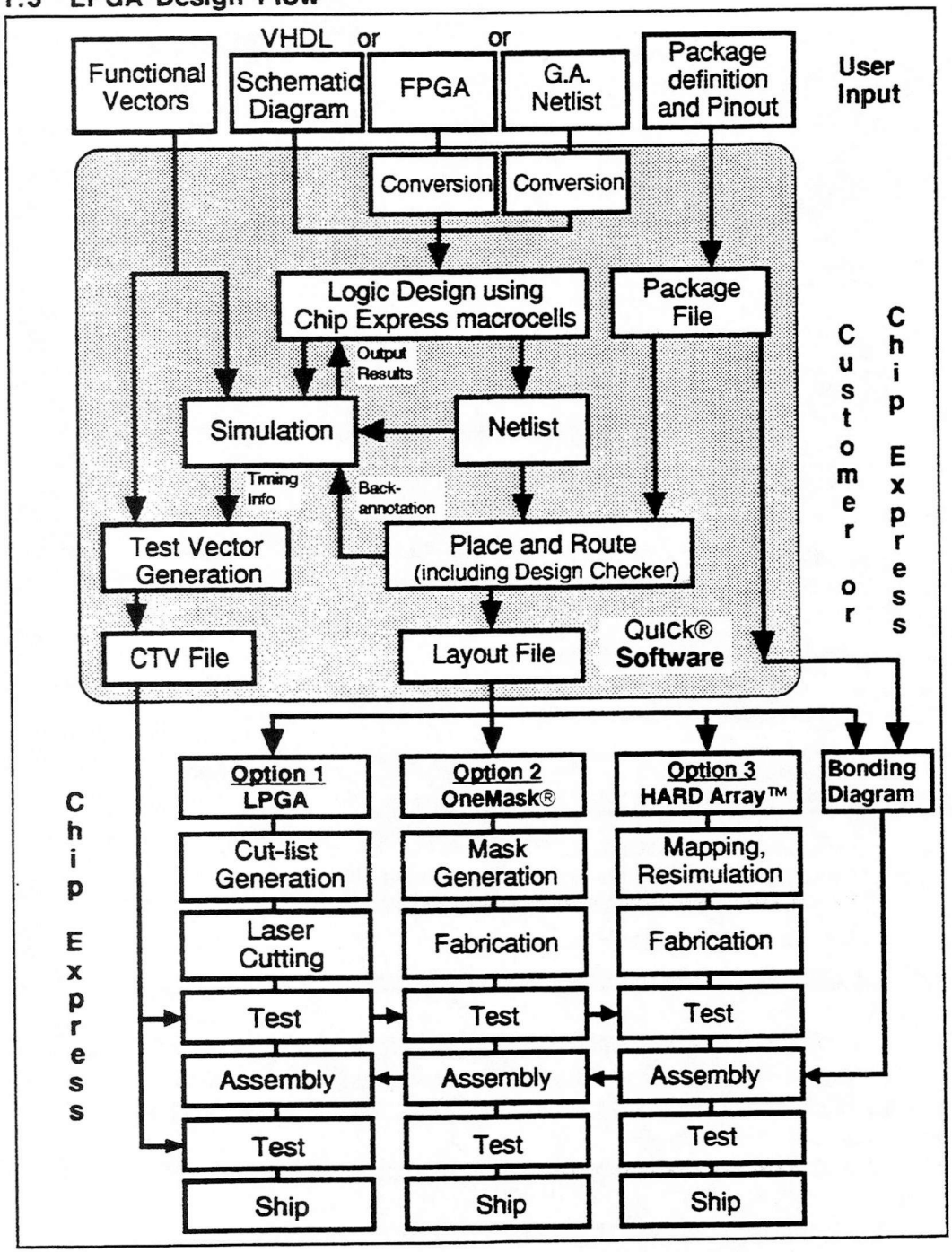
FPGA Conversions

Chip Express can convert FPGA designs to its LPGAs by using Exemplar and proprietary software. FPGA designs can be supported from AT&T, Actel, Altera, Quicklogic, and Xilinx. Please consult with the factory for any planned FPGA conversion.

Gate Array Conversions

Additionally, netlists may also be submitted in the libraries of the following gate array companies; AMI, Fujitsu, Hitachi, LSI Logic, NEC, OKI, Toshiba and VLSI Tech. Please consult with the factory regarding any planned gate array conversion.

1.3 LPGA Design Flow



2.1 LPGA Product Families

The QYH500 Family is state-of-the-art 0.8µ family and offers 300ps internal gate delay performance at higher gate counts.

The number of usable gates depends on the complexity of the design. However, in most cases, designs can achieve 70-90% utilization of the total gates, depending upon the architecture and logic type.

The following is a summary of primary characteristics of the QYH500 LPGA family:

0.8µ Typ. NAND delay = 300 ps Up to 16mA

Base Array	Raw Gates	% Utilization	Max. Bi-dir. I/Os	Number of Pads
QYH 510	10,100	70-90%	140	152
QYH 520	20,500	70-90%	204	224
QYH 530	29,800	70-90%	244	264
QYH 545	45,100	70-90%	300	320
QYH 580	80,100	50-60%	396	424

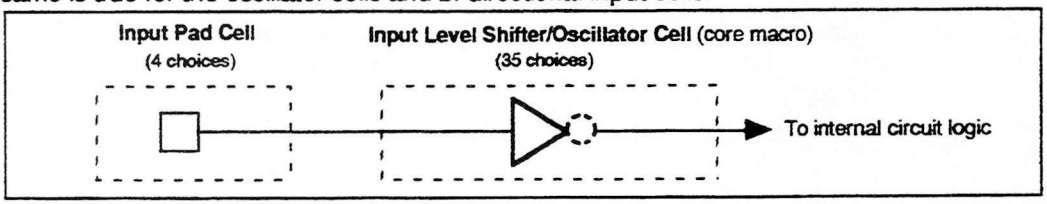
Cell Library Summary - QYH500 Family

375 I/O Buffers
82 Simple gates
69 Complex gates
57 Flip-flops
28 Latches

- Oscillators
- Clock Distribution Drivers
- Multiplexers, Decoders
- RAM Compilation

2.2 Input Cell Summary

The QYH500 series handles inputs somewhat differently than the QYH400 series. As shown below, each input level shifter cell must be paired with an input pad cell. The same is true for the oscillator cells and bi-directional input cells.



The following is a summary of the peripheral input cells available in the QYH500 Cell Library. This gives the designer a quick look at the types of input cells available. For detailed information, refer to the QYH500 Macrocell Library Databooks.

Input Pads

	Cell Name	# of Types	Input Macrocell Description	Fanout (inputs)	Typ.speed (ns)
1	IP D	1	Input pad w/PD	1	na
2	IP N	1	Input pad	1	na
3	IP U	1	Input pad w/PU	1	na
4	C OCIN	1	XTAL Oscillator Input Pad	1	na

Input Level-Shifter Core Macrocells

5	IP CBCx	4	CMOS Level Shifter	1, 2, 4, 8	0.43
6	IP CICx	4	Inv. CMOS Level Shifter	1, 2, 4, 8	0.75
7	IP HBCx	4	CMOS Level Shifter w/hyst	1, 2, 4, 8	0.80
8	IP HICx	4	Inv. CMOS Level Shifter w/hyst	1, 2, 4, 8	0.99
9	IP SBCx	4	TTL Level Shifter w/hyst	1, 2, 4, 8	1.60
10	IP SICx	4	Inv. TTL Level Shifter w/hyst	1, 2, 4, 8	1.52
11	IP TBCx	4	TTL Level Shifter	1, 2, 4, 8	1.45
12	IP TICx	4	Inv. TTL Level Shifter	1, 2, 4, 8	0.85

Oscillator Core Macrocells

13	C OC01	1	XTAL Oscillator Output	1	1.90
14	C OC02	1	XTAL Oscillator Output	2	0.96
15	C OC04	1	XTAL Oscillator Output	4	0.50
		39			

Notes : Typical speed column above shows the slowest of either tPD0 or tPD1.
w/hyst = with input hysteresis
w/PD = with Pull-Down resistor
w/PU = with Pull-Up resistor

2.3 Core Cell Summary

The following is a summary of the core logic cells available in the QYH500 Cell Library. This gives the designer a quick look at the types of logic cells available. For more detailed information, refer to the QYH500 Macrocell Library Databooks.

	Cell Name	# of Types	Core Macrocell Description		Fanout (inputs)	Notes
1	AD xxxx	11	AND Gate		1-2	
2	AN xxxx	10	AND-OR-INVERT		1	
3	AO xxxx	10	AND-OR		1-2	
4	CD QYx	6	Inverter Tree		50-2000	6 strengths
5	CX xxxx	4	Complex Functions		1-2	
6	DE xxxx	3	Decoder	Active HIGH	1	
7	DI xxxx	3	Decoder	Active LOW	1	
8	DFN xx	8	D-Flip-Flop	Neg. Edge	1-2	
9	DFP xx	8	D-Flip-Flop	Pos. Edge	1-2	
10	EN xxxx	3	Exclusive NOR		1-2	
11	EX xxxx	3	Exclusive OR		1-2	
12	IT xxxx	6	3-state buffer	Inverting	1-4	
13	IV xxxx	11	Inverter		1-30	11 strengths
14	JKN xx	8	JK-Flip-Flop	Neg. Edge	1-2	
15	JKP xx	8	JK-Flip-Flop	Pos. Edge	1-2	
16	LAN xx	8	Latch	Neg. Level	1-2	
17	LAP xx	8	Latch	Pos. Level	1-2	
18	LTP xx	4	Latch w/3S	Pos. Level	1	
19	MX xxxx	6	Multiplexer		1	
20	MI xxxx	6	Multiplexer	Inverting	1	
21	ND xxxx	16	NAND Gate		1-2	
22	NR xxxx	16	NOR Gate		1-2	
23	NT xxxx	6	3-State Buffer		1-4	
24	NV xxxx	11	Buffer Driver		1-30	11 strengths
25	OA xxxx	10	OR-AND		1-2	
26	ON xxx	10	OR-AND-INVERT		1	
27	OR xxxx	11	OR Gate		1-2	
28	SCN xx	4	Scan Flip-Flop	Neg. edge	1	
29	SCP xx	4	Scan Flip-Flop	Pos. Edge	1	
30	TFP xx	6	T-Flip-Flop	Pos. Edge	1-2	
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2.4 Output Cell Summary

The following is a summary of the peripheral output cells available in the QYH500 Cell Library. This gives the designer a quick look at the types of output cells available. For detailed information, refer to the QYH500 Macrocell Library Databooks.

	Cell Name	# of Types	Input	Output Description	Drive (mA)
1	O MDC —xx	2	—	CMOS Tri-state w/mslew w/PD	12, 16
2	O MDT —xx	2	—	TTL Tri-state w/mslew w/PD	12, 16
3	O MNC —xx	2	—	CMOS N-chan. OD w/mslew	12, 16
4	O MNT —xx	2	—	TTL N-chan. OD w/mslew	12, 16
5	O MOC —xx	2	—	CMOS N-chan. OD w/mslew w/PU	12, 16
6	O MOT —xx	2	—	TTL N-chan. OD w/mslew w/PU	12, 16
7	O MPC —xx	2	—	CMOS P-chan. OD w/mslew	12, 16
8	O MPT —xx	2	—	TTL P-chan. OD w/mslew	12, 16
9	O MQC —xx	2	—	CMOS P-chan. OD w/mslew w/PD	12, 16
10	O MQT —xx	2	—	TTL P-chan. OD w/mslew w/PD	12, 16
11	O MSC —xx	2	—	CMOS Tri-state w/mslew	12, 16
12	O MST —xx	2	—	TTL Tri-state w/mslew	12, 16
13	O MTC —xx	2	—	CMOS Totem pole w/mslew	12, 16
14	O MTT —xx	2	—	TTL Totem pole w/mslew	12, 16
15	O MUC —xx	2	—	CMOS Tri-state w/mslew w/PU	12, 16
16	O MUT —xx	2	—	TTL Tri-state w/mslew w/PU	12, 16

The above cells are moderate slew-rate-controlled.

17	O NDC —xx	6	—	CMOS Tri-state w/PD	2- 16
18	O NDT —xx	6	—	TTL Tri-state w/PD	2- 16
19	O NNC —xx	6	—	CMOS N-chan. OD	2- 16
20	O NNT —xx	6	—	TTL N-chan. OD	2- 16
21	O NOC —xx	6	—	CMOS N-chan. OD w/PU	2- 16
22	O NOT —xx	6	—	TTL N-chan. OD w/PU	2- 16
23	O NPC —xx	6	—	CMOS P-chan. OD	2- 16
24	O NPT —xx	6	—	TTL P-chan. OD	2- 16

The above cells are not slew-rate-controlled.

(con't.)

Notes :

-xx (Substitute xxmA output drive to complete macrocell name; 2, 4, 6, 8, 12 or 16)

w/hyst. = with input hysteresis
w/slew = with full slew-rate control
w/mslew = with moderate slew-rate control
w/PD = with Pull-Down resistor
w/PU = with Pull-Up resistor
OD = Open drain

2.4 Output Cell Summary (con't.)

	Cell Name	# of Types	Input	Output Description			Drive (mA)
25	O NQC —xx	6	—	CMOS P-chan. OD		w/PD	2- 16
26	O NQT —xx	6	—	TTL P-chan. OD		w/PD	2- 16
27	O NSC —xx	6	—	CMOS Tri-state			2- 16
28	O NST —xx	6	—	TTL Tri-state			2- 16
29	O NTC —xx	6	—	CMOS Totem pole			2- 16
30	O NTT —xx	6	—	TTL Totem Pole			2- 16
31	O NUC —xx	6	—	CMOS Tri-state		w/PU	2- 16
32	O NUT —xx	6	—	TTL Tri-state		w/PU	2- 16

The above cells are not slew-rate-controlled.

33	O SDC —xx	6	—	CMOS Tri-state	w/slew	w/PD	2- 16
34	O SDT —xx	6	—	TTL Tri-state	w/slew	w/PD	2- 16
35	O SNC —xx	6	—	CMOS N-chan. OD	w/slew		2- 16
36	O SNT —xx	6	—	TTL N-chan. OD	w/slew		2- 16
37	O SOC —xx	6	—	CMOS N-chan. OD	w/slew	w/PU	2- 16
38	O SOT —xx	6	—	TTL N-chan. OD	w/slew	w/PU	2- 16
39	O SPC —xx	6	—	CMOS P-chan. OD	w/slew		2- 16
40	O SPT —xx	6	—	TTL P-chan. OD	w/slew		2- 16
41	O SQC —xx	6	—	CMOS P-chan. OD	w/slew	w/PD	2- 16
42	O SQT —xx	6	—	TTL P-chan. OD	w/slew	w/PD	2- 16
43	O SSC —xx	6	—	CMOS Tri-state	w/slew		2- 16
44	O SST —xx	6	—	TTL Tri-state	w/slew		2- 16
45	O STC —xx	6	—	CMOS Totem pole	w/slew		2- 16
46	O STT —xx	6	—	TTL Totem Pole	w/slew		2- 16
47	O SUC —xx	6	—	CMOS Tri-state	w/slew	w/PU	2- 16
48	O SUT —xx	6	—	TTL Tri-state	w/slew	w/PU	2- 16

The above cells are full slew-rate-controlled.

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Notes:
-xx (Substitute xxmA output drive to complete macrocell name;
2, 4, 6, 8, 12 or 16)
w/hyst. = with input hysteresis
w/slew = with slew rate control
w/PD = with Pull-Down resistor
w/PU = with Pull-Up resistor
OD = Open drain

2.4 Output Cell Summary (con't.) - Bi-directional Cells

The following is a summary of the bi-directional cells available in the QYH500 Cell Library. This gives the designer a quick look at the types of bi-directional cells available. For detailed information, refer to the QYH500 Macrocell Library Databooks. Note that in the QYH500 series, a separate input-level-shifter cell must be selected to be used with each bi-directional cell.

	Cell Name	# of Types	Output Description				Drive (mA)
1	BM NCU —xx	2	CMOS Buffer	N-chan. OD	w/mslew	w/PU	12, 16
2	BM NTU —xx	2	TTL Buffer	N-chan. OD	w/mslew	w/PU	12, 16
3	BM PCD —xx	2	CMOS Buffer	P-chan. OD	w/mslew	w/PD	12, 16
4	BM PTD —xx	2	TTL Buffer	P-chan. OD	w/mslew	w/PD	12, 16
5	BM TCD —xx	2	CMOS Buffer	Tri-state	w/mslew	w/PD	12, 16
6	BM TCN —xx	2	CMOS Buffer	Tri-state	w/mslew		12, 16
7	BM TCU —xx	2	CMOS Buffer	Tri-state	w/mslew	w/PU	12, 16
8	BM TTD —xx	2	TTL Buffer	Tri-state	w/mslew	w/PD	12, 16
9	BM TTN —xx	2	TTL Buffer	Tri-state	w/mslew		12, 16
10	BM TTU —xx	2	TTL Buffer	Tri-state	w/mslew	w/PU	12, 16
			The above cells are moderate slew-rate-controlled.				
11	BN NCU —xx	6	CMOS Buffer	N-chan. OD		w/PU	2- 16
12	BN NTU —xx	6	TTL Buffer	N-chan. OD		w/PU	2- 16
13	BN PCD —xx	6	CMOS Buffer	P-chan. OD		w/PD	2- 16
14	BN PTD —xx	6	TTL Buffer	P-chan. OD		w/PD	2- 16
15	BN TCD —xx	6	CMOS Buffer	Tri-state		w/PD	2- 16
16	BN TCN —xx	6	CMOS Buffer	Tri-state			2- 16
17	BN TCU —xx	6	CMOS Buffer	Tri-state		w/PU	2- 16
18	BN TTD —xx	6	TTL Buffer	Tri-state		w/PD	2- 16
19	BN TTN —xx	6	TTL Buffer	Tri-state			2- 16
20	BN TTU —xx	6	TTL Buffer	Tri-state		w/PU	2- 16
			The above cells are not slew-rate-controlled.				
21	BS NCU —xx	6	CMOS Buffer	N-chan. OD	w/slew	w/PU	2- 16
22	BS NTU —xx	6	TTL Buffer	N-chan. OD	w/slew	w/PU	2- 16
23	BS PCD —xx	6	CMOS Buffer	P-chan. OD	w/slew	w/PD	2- 16
24	BS PTD —xx	6	TTL Buffer	P-chan. OD	w/slew	w/PD	2- 16
25	BS TCD —xx	6	CMOS Buffer	Tri-state	w/slew	w/PD	2- 16
26	BS TCN —xx	6	CMOS Buffer	Tri-state	w/slew		2- 16
27	BS TCU —xx	6	CMOS Buffer	Tri-state	w/slew	w/PU	2- 16
28	BS TTD —xx	6	TTL Buffer	Tri-state	w/slew	w/PD	2- 16
29	BS TTN —xx	6	TTL Buffer	Tri-state	w/slew		2- 16
30	BS TTU —xx	6	TTL Buffer	Tri-state	w/slew	w/PU	2- 16
		140	The above cells are full slew-rate-controlled.				

Notes : -xx (Substitute xxmA output drive to complete macrocell name; 2, 4, 6, 8, 12 or 16)
w/hyst. = with input hysteresis w/PD = with Pull-Down resistor
w/slew = with slew rate control w/PU = with Pull-Up resistor OD = Open drain

2.5 PCI Bus Compatibility

New designs, used for the PCI bus architecture, need the ability to have buffers compatible with the PCI specification. The PCI spec defines the boundaries a PCI buffer must operate within. This spec defines the complete bus behavior. Compatibility to it assures proper operation of the system.

Two QYH500 output buffers were checked for PCI compatibility, the BNTTN12 and BNTTN16. These buffers were simulated with both Yamaha and Tower fabs' extracted process data. The buffers were checked for their I/V curve, and their driving slew-rate. Future checks will include PCI-Speedway simulation as a reference.

The chart below shows the results of those tests:

	Yamaha Fab QYH500	Tower Fab QYH500
BNTTN12	I/V - Fail Slew-rate - OK	I/V - OK* Slew-rate - OK
BNTTN16	I/V - OK Slew-rate - OK**	I/V - OK Slew-rate - OK**

* Results from graphs, pass on the edge.

** Spec is 1V/ns - 5V/ns, with fail at 5.2V/ns. The simulation was run without package parasitics, which slow down the slew-rate.

No simulations were run with overshoot/ undershoot beyond the rail voltages. In real life, this might be a reliability issue, something which we cannot observe in simulations.

Our buffer's input capacitance is 9pf. This does not include package parasitics. The PCI spec specifies a maximum load of 10pf., which may be a problem in certain packages.

2.6 DC Specifications

Absolute Maximum Ratings

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{CC}	Supply Voltage		-0.3	6.7	V
V_I	Input Voltage		-0.3	Vcc+0.3	V
V_{ESD}	Electro-static Discharge	Human body model	-2000	2000	V
I_{OS}	Output Shorted	<5 seconds, 1 output at a time	-100	100	mA
T_S	Storage Temperature	No power applied	-55°	+125°	°C

Reliability may be affected if parts are operated at Absolute Maximum values.

Recommended Operating Conditions

Symbol	Parameter	Conditions	MIN	NOM	MAX	Unit
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
V_I	Input Voltage		0V		Vcc	V
T_A	Operating Temp. (Com.)	Over Vcc range	0°	25°	70°	°C
T_A	Operating Temp. (Ind.)	Over Vcc range	-40°		85°	°C

DC Characteristics

(Over Recommended Operating Conditions)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Lo-Level Input Voltage	CMOS Input			0.3 Vcc	V
	without hysteresis	TTL Input			0.8	
V_{IH}	Hi-Level Input Voltage	CMOS Input	0.7 Vcc			V
	without hysteresis	TTL Input	2.0			
V_{HYS}	Input Hysteresis	CMOS Input		1.36		V
V_{TH+}	Input High Threshold		2.64			
V_{TH+}	Input Low Threshold				1.71	
V_{HYS}	Input Hysteresis	TTL Input		0.47		V
V_{TH+}	Input High Threshold		1.56			
V_{TH+}	Input Low Threshold				1.37	
V_{OL}	Output Voltage LOW	Iol = 2, 4, 8, 12, 16mA			0.4	V
V_{OH}	Output Voltage HIGH	Ioh=-2, -4, -8, -12, -16mA	Vcc-1			V
I_{OL}	Output Current LOW	Vol = 0.4V	+2 to 16			mA
I_{OH}	Output Current HIGH	Voh= Vcc- 1.0V	-2 to -16			mA
I_{LI}	Input Leakage Current	Vin = 0 to 5.0V	-10		10	µA
I_{LO}	Output Leakage Curr.	Vout= 0 to 5.0V.	-10		10	µA

3.1 Gate Array Selection

Various factors affect the selection of a suitable base gate array. Among these are the following :

Technology Selection

	500 Series candidates
Density	If density is the over-riding factor, select from the 500 series. For gate-limited designs.
Max. I/O	If max. I/Os is the over-riding factor, select from the 500 series. For I/O-limited designs.
DPLL	If a Digital Phase-Locked-Loop is required, select from the 500 series.
RAM	If a large RAM is required, select from the 500 series.
Speed	If speed is the over-riding factor, select from the 500 series.

Package Selection

Match	Select the package which provides the best "match" to a given array, i.e., required pins and available pads are approximately equal.
Power	If high power dissipation is an issue, select the die-package package combination which provides for maximum heat dissipation.
Support	Select a die-package combination which is supported in BOTH the prototype option, and the production option. It is easier and cheaper to utilize die-package combinations which are characterized, and well known.

Obviously, the designer would like to achieve the best of all worlds. But in reality, compromises must be made because of cost, speed, etc. The above list merely makes suggestions, around which trade-offs will be made for the individual situation.

3.2 Package Selection (Prototype)

LPGA Array-Package Match-ups for the QYH500 Family

Chip Express supports the following prototype combinations of package and die. For production package support, please consult the factory.

	Base Array :	QYH 510	QYH 520	QYH 530	QYH 545	QYH 580
Dual In Line	24-DIP	X	X			
	28-DIP	X	X			
	32-DIP	X	X	X		
	40-DIP	X	X	X		
	48-DIP	X	X	X		
	64-SDIP	X				
Leadless Chip Carrier						
	44-LCC	X	X	X		
	68-LCC	X	X	X		
	84-LCC	X	X	X	X	
Quad Flat Pack						
	44-QFP					
	64-QFP	X	X			
	80-QFP	X	X			
	100-QFP	X	X			
	120-QFP	X	X	X	X	X
	128-QFP	X	X	X	X	X
	144-QFP	X	X	X	X	X
	160-QFP		X	X	X	X
	208-QFP		X	X	X	X
	208-QFPL					
	240-QFP			X	X	X
	304-QFP				X	X
Square Quad Flat Pack						
	64-SQFP					
	100-SQFP	X	X			
	144-SQFP	X	X	X	X	
	176-SQFP		X	X	X	
	208-SQFP		X	X	X	X
Pin Grid Array						
	69-PGA	X	X	X		
	100-PGA	X	X	X		
	132-PGA	X	X	X	X	
	144-PGA	X	X	X	X	
	180-PGA		X	X	X	
	208-PGA		X	X	X	
	224-PGA		X	X	X	X
	256-PGA			X	X	
	299-PGA				X	X
Ball Grid Array						
	352-BGA	X	X	X	X	X

3.3 Package Power Consumption (Plastic)

Maximum Plastic-Package Power Consumption for the QYH500 Family

The chart below lists the maximum power consumption for the given production plastic package/ QYH500 die combinations. For other packages, please consult the factory.

	Base Array :	QYH 510	QYH 520	QYH 530	QYH 545	QYH 580
Dual In Line	24-DIP	500	X	X	X	Y
	28-DIP	500	X	X	X	Y
	32-DIP	500	500	X	X	Y
	40-DIP	500	500	X	X	Y
	48-DIP	X	X	X	X	Y
	64-SDIP	X	X	X	X	Y
Plastic Leaded Chip Carrier						
	44-PLCC	X	X	X	X	Y
	68-PLCC	550	550	550	X	Y
	84-PLCC	650	650	650	X	Y
Quad Flat Pack						
	44-QFP	500	X	X	X	Y
	64-QFP	500	X	X	X	Y
	80-QFP	500	500	X	X	Y
	100-QFP	500	500	X	X	Y
	120-QFP	X	X	X	X	Y
	128-QFP	650	650	650	X	Y
	144-QFP	650	650	650	650	Y
	160-QFP	650	650	650	650	Y
	208-QFP	650	650	650	650	Y
	208-QFPL	650	650	650	650	Y
	240-QFP	650	650	650	650	Y
	304-QFP	X	X	X	X	Y

Notes :

X = Denotes package combinations not available

Y = The QYH580 is packaged only in ceramic packages.

4.1 Overview

The LPGA design methodology is basically the same as conventional CMOS logic design methodology. However, please pay special attention to the following items.

4.2 Worst-Case Design

Variations in delay characteristics which are caused by variations in manufacturing processes cannot be compensated for after chip completion. Thus, a design which considers worst-case delay characteristics should be used.
Examples of typical derating factors:

Min.	Nom.	Max.
0.55x	1.0	1.7x

Maximum worst case delay in CMOS occurs at

Low supply voltage = 4.75 Volts (derate nominal ≈ 20-30%),
High ambient temperature = 70°C (derate nominal ≈ 30-40%),
Worst case process = 10% (derate nominal ≈ 10-20%).

4.3 Macrocell Usage

To incur minimum cost, the customer should create the schematic design using the LPGA cells provided in the cell library. If the customer submits a netlist from a major FPGA or gate array manufacturer, Chip Express can convert the macros used into Chip Express macros for an additional fee. Chip Express would prefer that the customer simulate the design with back-annotation, using Chip Express tools, before any production begins.

4.4 Power Consumption

There are some restrictions for power consumption vs. chip size. The least number of gates and routing should be used to achieve the required functions. In CMOS, higher frequencies of operation require higher power.

Although Chip Express arrays are CMOS logic arrays, and as such do not consume static supply current, they do have a finite average power consumption caused by transient currents during switching. This average power consumption increases with clock frequency, and can reach up to 1-2 Watts for the larger arrays and higher frequencies.

Every package is characterized by its ability to dissipate power, and typically, for a device with a 1 Watt average power consumption, the temperature difference between the chip and the outside air can be between 35°C to 45°C. For a 70°C outside temperature, this brings the chip temperature up to 120°C. Chip Express internally defines the maximum acceptable temperature for a reliable device operation, and specifies a maximum power consumption for every package. Please refer to the package tables for the maximum values.

4.4 Power Consumption (con't.)

In some cases, the use of a heat sink on the package is recommended, and will improve the heat transfer from the chip to the outside air. Another method of heat transfer is to use a fan in the system chassis. Please consult Chip Express to find the temperature coefficient for the package under these conditions, so that the chip temperature (junction temperature) can be calculated.

Power Dissipation Estimation
The power dissipation in CMOS devices is mainly due to four different sources:

- Base array static power caused by leakage which is essentially negligible in CMOS devices,
- DC currents in pull-up and pull-down circuits and in RAMs,
- Overlap currents which exist during transitions when both N and P transistors are conducting,
- Charging and discharging of circuit capacitance, which consists of macrocell capacitance, interconnect capacitance, and output load capacitance.

The overlap current and the power dissipated during transitions of the core cells depend on the gate count as well as on the average transition frequency, i.e., on clock frequency multiplied by the fraction of cell outputs which change every cycle. This fraction may be estimated, or a 20% default value may be used. Futhermore, the overlap current will depend on the signal transition time for each macrocell. An average transition time of 1.5ns will be assumed.

A more accurate estimation of the dissipated power may be made when latches, flip-flops, and RAMs are treated separately from random logic cells. An estimation for the power dissipated by these cells depends on their number, as well as on the average frequency at which the data changes.

The power dissipated by output cells depends essentially on the output load driven by those cells, and on the output frequency.

The power dissipated by pull-ups and pull-downs depends on the fraction of the time in which these cells sink current. This fraction should be estimated by the designer.

I/O Pins
A power supply pad pair is needed for every 64mA of output current.

4.4 Power Consumption (con't.)

Power Estimation Formulas

- Pull-ups

$$P_{pu}(mW) = 0.22 \times N_{pu} \times P_{pu}$$

where, N_{pu} is the number of pull-ups in the design, and
P_{pu} is the average fraction of the time for which the pull-ups consume current.

- Pull-downs

$$P_{pd}(mW) = 0.3 \times N_{pd} \times P_{pd}$$

where, N_{pd} is the number of pull-downs in the design, and
P_{pd} is the average fraction of the time for which the pull-downs consume current.

- Output Buffers

$$P_{outb}(mW) = 0.028 \times \sum N_i \times f_{outb}(i) \times (10 + C_{package} + C_{load})$$

where, N_i is the number of output buffers with an output frequency $f_{outb}(i)$[MHz.],
$C_{package}$ is the package capacitance per pin, and
C_{load} is the average capacitance of the outside load.

- Core Logic Cells

$$P_{logic}(mW) = 0.014 \times \sum N_{gates}(i) \times f_c(i) \times P_c(i)$$

where, the sum is over all the clocks,
$N_{gates(i)}$ is the number of gates associated with clock #i in the design,
$f_c(i)$ is the clock frequency for clock #i, and
$P_c(i)$ is the percentage of gates changing for each clock cycle, which may be estimated by the designer, or a default value of 20% may be used.

- Flip-Flops and Latches

$$P_{ff}(mW) = 0.024 \times \sum N_i \times f_{clk}(i) + 0.031 \times \sum N_i(i) \times f_{out}(i)$$

where, N_i is the number of flip-flops and latches connected to clock driver #i, with a clock,
$f_{clk}(i)$ is the clock frequency for clock driver #i [MHz.], and
$f_{out}(i)$ is the output frequency of the flip-flops, (i.e., $f_{clk}(i)$ = the fraction of flip-flops toggling each clock cycle). $f_{out}(i)$ may be estimated by the designer, or a default value of 0.25 may be used.

4.4 Power Consumption

Power Estimation Formulas (con't.)

• RAMs

The power dissipated in a RAM has a DC component whose source is the sense amplifiers in the RAM, and a frequency dependent component whose source is the pre-charging of the bus lines. The dissipated power estimation for an M-word x N-bits-per-word RAM, operating at a frequency f[MHz.], is given in the formulas below:

For a Single-port RAM, $P_{ram}[mW] = 2.8 \times N + 0.0012 \times f[MHz.] \times M \times N$

For a Dual-port RAM, $P_{ram}[mW] = 5.6 \times N + 0.0024 \times f[MHz.] \times M \times N$

For a FIFO RAM, $P_{ram}[mW] = 2.8 \times N + 0.0024 \times f[MHz.] \times M \times N$

Total Power Estimation

The total power dissipation is given by:

$$P_{total}(mW) = P_{pu} + P_{pd} + P_{outb} + P_{logic} + P_{ff} + P_{ram}$$

Derivation of Power Estimation Formulas

Pull-ups

The estimate is based on a DC current of 40µA derived from a SPICE simulation of the QYH500 pull-down macro, and on the assumption that Vdd=5.25V.

Pull-downs

The estimate is based on a DC current of 55µA derived from a SPICE simulation of the QYH500 pull-down macro, and on the assumption that Vdd=5.25V.

Output Buffers

The estimate is based on the assumption that Vdd=5.25V. The capacitance of the output pad is 10pf.

Core Logic Cells

The estimate is based on SPICE simulations with an input rise/fall time of 1.5ns, and with an average interconnect load of 0.047pf per input pin. The accuracy of the simulation has also been verified experimentally ("Power" application) for logic chains with a small amount of interconnect, and an input rise/fall time of less than 0.5ns.

Flip-Flops and Latches

The estimate for flip-flops with data toggling is based on measurements ("Power" application and "Skew" application) and corresponds well to the SPICE results for a clock rise/fall time of 3ns. The estimate for a flip-flop with constant data has been derived from a SPICE simulation.

RAMs

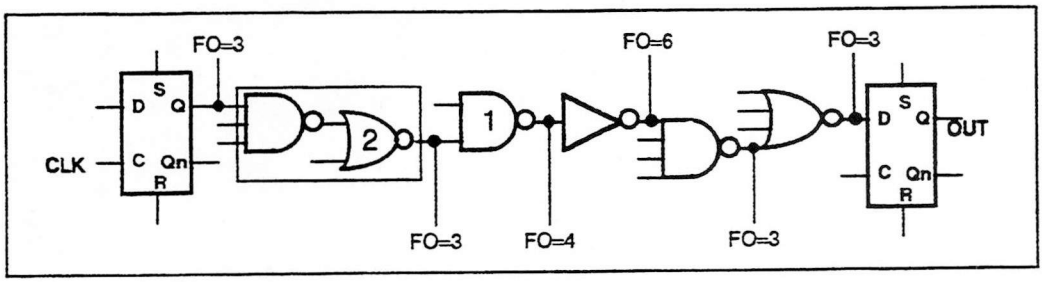
The estimate is based on SPICE simulations. A clock duty cycle of 50% is assumed, and the data is assumed to be "1" and "0", an equal percent of the time. The DC current in the sense amplifier is 2.1mA when the clock is low, and the data is "1". Otherwise, it is zero. The pre-charge current is assumed to be proportional to the clock frequency, and low enough for complete recharging of the bus lines.

4.5 Operation Speed - Maximum Frequency Considerations

The operating speed is verified by timing simulation, after the placement and routing of the chip. The operating speed, especially any critical paths, should be considered in the design.

When the Chip Express array is selected for a design, evaluate the maximum frequency of operation. Typically, each design will contain one or more critical paths which need to be examined, to make sure that the choice of technology (1.2µ or 0.8µ) is optimal for the application.

The most common critical path consists of a string of gates between 2 registers, as shown in the example below :



We have to consider the following delay :

$$t_{path} = t_{pdh}\text{ (Clk. to Q)} + \sum\text{all gate delays} + t_{setup}\text{ (Data-in to Clk)}$$

Let us assume that the QYH400 cell library gives a total delay for this path of :

$$t_{path} = 24.5\text{ns worst case}$$

The maximum frequency is :

$$f_{max} = 1 / 24.5\text{ns} = 40.8\text{ MHz.}$$

If the design is supposed to run at 50MHz., we must try the QYH500 cell library. This 0.8µ technology provides for the same path :

$$t_{path} = 16.6\text{ns worst case}$$

The maximum frequency is now :

$$f_{max} = 1 / 16.6\text{ns} = 60\text{ MHz.}$$

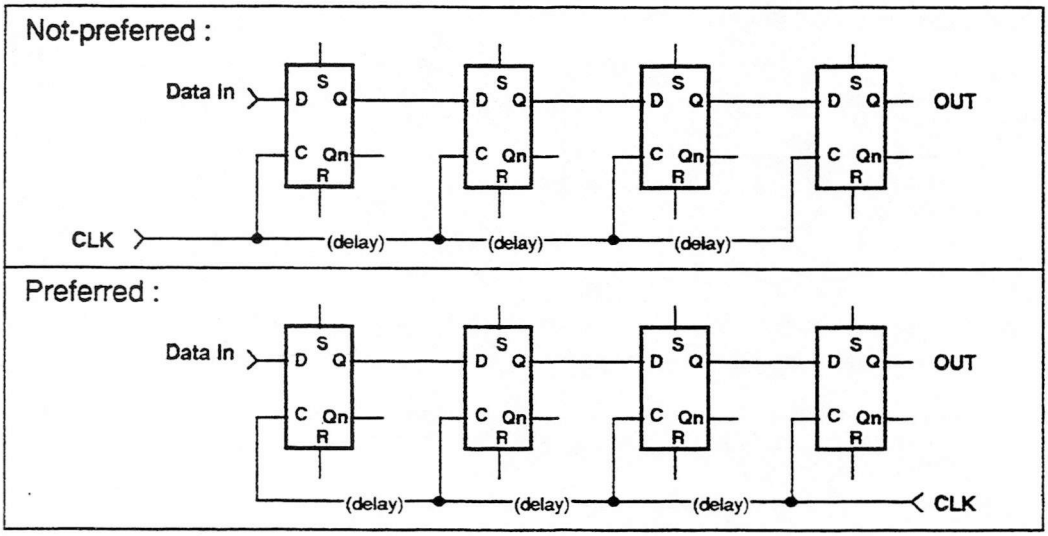
Therefore, the design must use the QYH500 family to meet the speed requirements.

4.5 Operation Speed (con't.)

CLOCK SKEW

Definition of clock skew : the clock skew is the phase shift, or delay, between 2 clock signals from the same source, going into any of 2 different flip-flops in the array.

Referring to the critical path shown below, the first shift register shown can malfunction, if there is too much delay between the clock inputs. Data can race from one F/F to the next, before the clock arrives. By clocking the second shift register from back-to-front, the delay helps to maintain functionality, by clocking in the opposite direction.



The clock skew is caused by a difference in the clock delay between the clock input pad, and any 2 registers in the array. Usually, the bigger the clock network, the longer the clock delay, and the larger the skew.

Chip Express has a layout scheme for the clock network that minimizes clock skew. The scheme consists of building an equal number of clock buffers between the clock pad, and any register in the design. The clock network interconnect is also carefully balanced to equalize capacitive loading on all the clock buffers.

The following pages outline the Chip Express methodology for the clock network design and layout.

4.5 Operation Speed (con't.)

CLOCK NETWORK

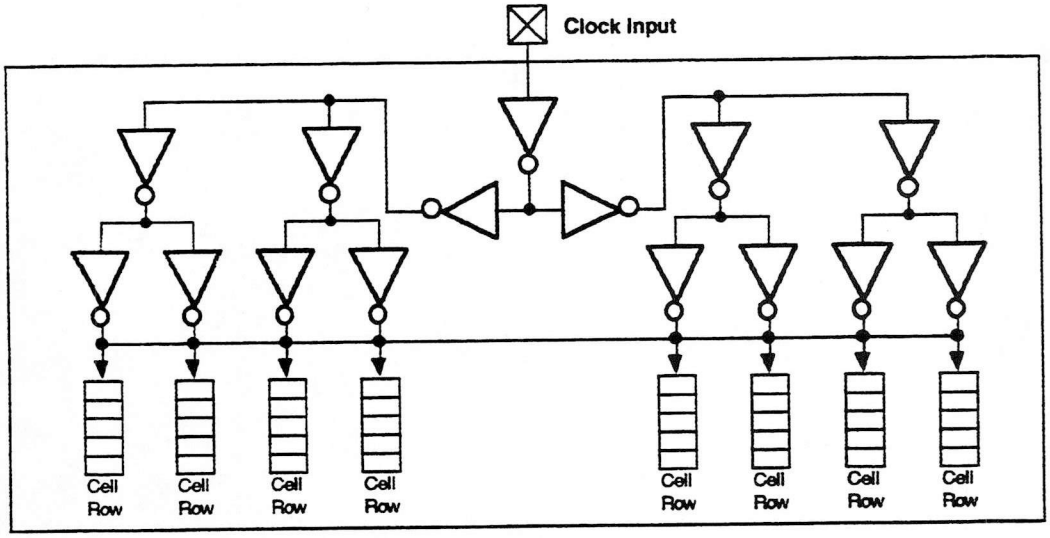
There are many types of clock distribution schemes : clock trunk, clock grid or mesh, clock loop, etc. Chip Express recommends using a clock tree scheme which minimizes clock skew.

A clock tree consists of a number of branches where each branch has one buffer driving 2 branches. At the clock input pad, there is one buffer which drives 2 branches, which then generate 4 branches, then 8 branches, and so on, until there are enough branches to provide for one clock driver per cell-row in the array. The size of the clock tree depends on the number of flip-flops to be driven (see example).

The delay between the clock input pad and any flip-flop, remains approximately the same; therefore, the clock skew is minimized.

The larger the number of flip-flops, the larger the number of branches needed, and the larger the overall clock delay between the clock input pad, and the flip-flop clock inputs. Smaller clock trees have 4 stages, and larger clock trees have 6 stages. Note that the last stages are shorted together to minimize any skew.

Example of a clock tree for 8 cell rows :



4.5 Operation Speed

CLOCK NETWORK (con't.)
Chip Express builds a clock network automatically, once a clock buffer macro has been selected. These macros are "soft-macros", made up of standard library cells, but the placement of each cell is semi-fixed, and determined by the cell placement software.

There are 6 clock buffer macros presently available to drive from a dozen to over 2,500 flip-flops, called CDQY1 through CDQY6. To determine what clock buffer macrocell to choose for a particular design in the QYH500 Family, use the following table :

	# of Levels	# of Flip-flops to be driven	
		MIN.	MAX.
CDQY-1	2	50	100
CDQY-2	2	100	250
CDQY-3	4	250	450
CDQY-4	4	450	750
CDQY-5	6	750	1,500
CDQY-6	6	1,500	2,500

In the example, we have selected a clock tree with 4 levels. The corresponding clock buffer macro is CDQY4. To minimize the skew generated by the clock tree, all level n buffers have their outputs shorted together.

Note that the clock buffer macros all have an even number of buffer levels, so that the resultant clock output signal into the flip-flops has a 50% duty cycle, and is non-inverting.

4.5 Operation Speed

CLOCK NETWORK (con't.)
The clock delay introduced by the macrocell, can be derived from the cell library information, assuming an approximate interconnect load, or can be computed by the logic simulation using back-annotated loads.

The following table compares maximum clock skews, and clock delays, for the clock buffer macrocells in the QYH500 technology :

	QYH500 Family Arrays		
	MAX F/Fs	MAX Delay	MAX Skew
CDQY-1	up to 100	2 ns	1.5 ns
CDQY-2	up to 250	2 ns	1.5 ns
CDQY-3	up to 450	3 ns	1.5 ns
CDQY-4	up to 750	3 ns	1.5 ns
CDQY-5	up to 1,500	3 ns	1.5 ns
CDQY-6	up to 2,500	3 ns	1.5 ns

Conditions : Vdd=4.75 to 5.25V, T°= 0° to 70°C

Typically, the clock skew is minimized to be less than 1ns throughout the array. However, the clock delay between the clock input pad, and the FF inputs, can be quite large, between 5 and 10ns, and will reduce the amount of time available for the data to exit the chip, and reach another chip clocked by the same clock on the PC board. To reduce that delay, a digital phase-locked-loop (DPLL) can be used.

A phase-locked-loop is a macrocell in the Chip Express library which reduces or eliminates the internal clock delay. It does so by comparing the delay between the clock, as seen by a remote FF on the chip (remote clock), and the incoming clock at the clock pad (incoming clock).

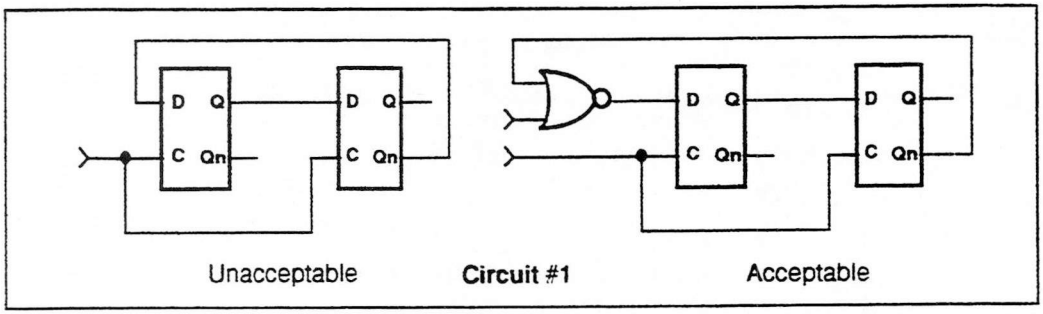
As long as the remote clock is delayed with respect to the incoming clock, the DPLL will regenerate a new clock signal that is ahead of the incoming clock. The DPLL achieves this by running the incoming clock through a delay line that is longer than 1 clock period. The DPLL then selects a point in the delay line that will provide enough of an advance on the next clock edge, to compensate for the clock tree delay. Please refer to the DPLL application note in Chapter 7.

This DPLL does not require any external components. It is available for all QYH500 family arrays.

4.6 Initialization

After power is applied, the logic states of the latches, flip-flops, and RAM (if present) are unknown. The logic must then be initialized with test vectors; otherwise, the design is not testable. During logic simulation, logic states are also undefined at t=0. As a consequence, the register cells in the array have to be initialized step-by-step, until all logic storage elements are in a known state.

The figure below shows examples of acceptable and unacceptable circuits.



# of Test Vectors

Since the number of test vectors is limited, efficient initialization is absolutely essential. Consequently, flip-flops, memories, and counters need a well-organized test circuit, so that the entire circuit can be cleared by a single pulse, or just a few steps.

Splitting of Test Vectors

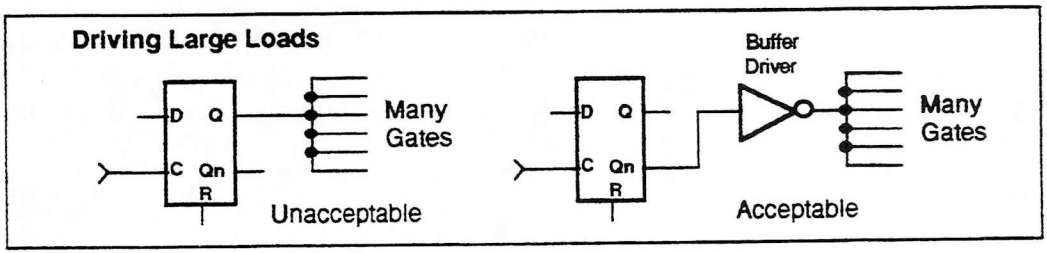
It may be convenient to separate the whole circuit into a number of blocks, and prepare the test vectors accordingly. However, even in this case, it is still recommended that the entire circuit be initialized in the first group of vectors. If some portions of the logic remain uninitialized, problems may result when designing the test vectors for another section. Initialization of the entire circuit can help to minimize the steps, since the portions which are not being tested may be operating.

4.7 Drivability

4.7.1 Driving Heavy Loads

When driving heavy loads, it is desirable to use a strong driver. For example, the output of a flip-flop may go to the inputs of 30 gates. Since a flip-flop does not have high drive capability, the signal level on the node will change very slowly. This causes slow rise and fall times, which slow the speed of the circuit, reduces noise immunity, and causes high current consumption.

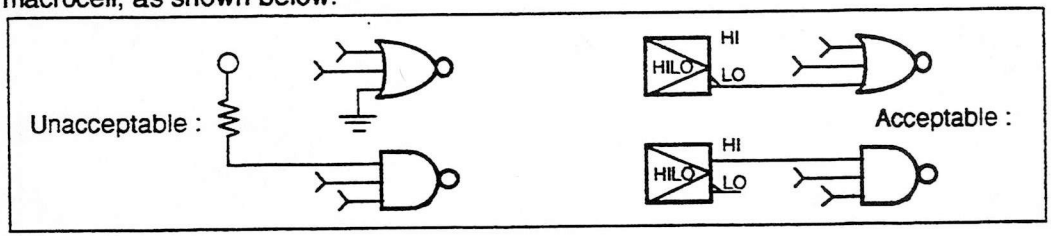
In order to overcome this problem, drive is "built-up", by inserting additional buffers between the flip-flop output and the gate inputs. Although additional delay elements are being introduced, the faster rise and fall times result in much faster operation, reduced noise susceptibility, and reduced current consumption. Splitting nets should help as well.



4.8 Design Do's and Don'ts

4.8.1 Unused Input Pins

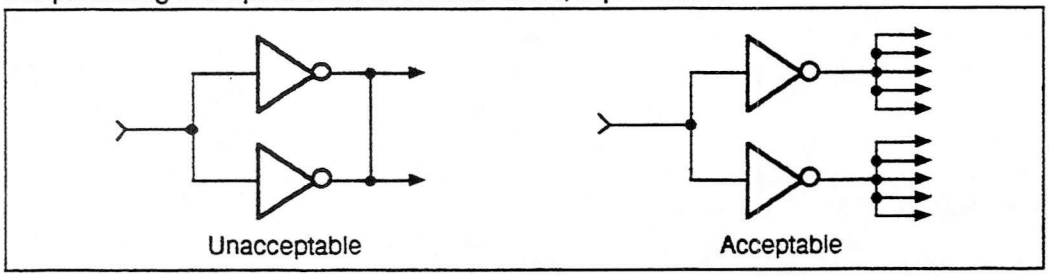
In CMOS technology, it is not permissible to leave any input pins floating. The pins will float to, and remain at, the input threshold voltage. The slightest noise will cause undesired switching to occur. In some technologies, vendors specify that unused inputs be tied to Vcc or Ground. In the QYH500 family, tie the unused inputs to a "HILO" macrocell, as shown below.



4.8 Design Do's and Don'ts (con't.)

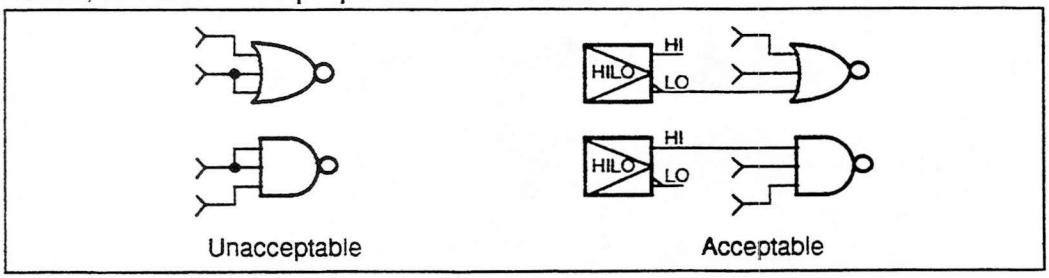
4.8.2 Parallel Output Cells

The paralleling of output buffers to increase drive, is prohibited.



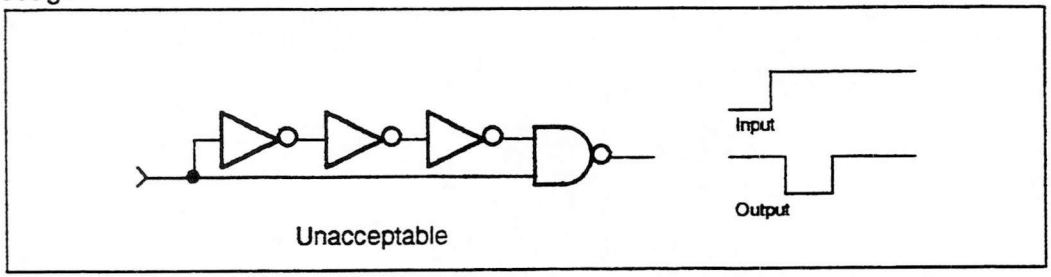
4.8.3 Tying Inputs Together

On any given gate, two or more input pins should not be driven by the same input signal. Instead, tie the unused input pins to a HILO macrocell.



4.8.4 Chopper Circuit (gate-delay one-shot)

The one-shot waveform, which is generated by the delay of a gate(s), does not provide a stable pulse width, due to manufacturing variations. Thus, it cannot be used in the logic design.

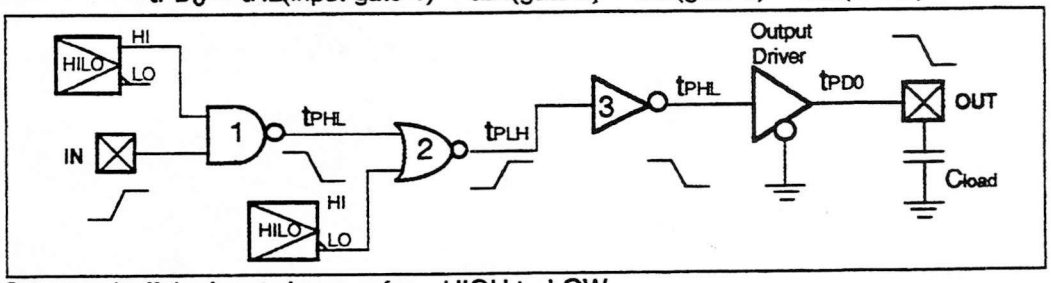


4.9 Propagation Delay

4.9.1 Calculation of Device Delay Time

The propagation delay time from input to output for a selected path can be calculated, as the summation of delays of each element in the delay path, using the equations below; For the example below, if the input changes from LOW to HIGH,

$$t_{PD0} = t_{HL(\text{input gate 1})} + t_{LH(\text{gate 2})} + t_{HL(\text{gate 3})} + t_{HL(\text{driver})}$$



Conversely, if the input changes from HIGH to LOW,

$$t_{PD1} = t_{LH(\text{input gate 1})} + t_{HL(\text{gate 2})} + t_{LH(\text{gate 3})} + t_{LH(\text{driver})}$$

After calculation, use the greater t_{PD} value as the propagation delay time for the path.

4.9.2 Delay Calculations of Core Cell Nets

The output response of a CMOS core macrocell is equivalent to the charge and discharge model of the load capacity. The delay time for the net is the sum of the cell internal delay and the load delay. The following are the equations for the delay time of a core cell output net;

$$D_{[s]} = Di + Dt + Dc_{[s]}$$

where,

D = total delay of the gate and net, from the input of the driving gate, through the net segment, to the input port of the driven gate

Di = intrinsic gate delay, t_{PLH} and t_{PHL}, given in the macrocell databook

Dt = total loading delay plus the total routing delay of the net

= Δt_{PLH} (Cwires + Cinputports)

= Δt_{PHL} (Cwires + Cinputports)

where Δt_{PLH} and Δt_{PHL} are given in the macrocell databook in ns/pf.

Cwires = the total wire capacitance of the net

Cinputports = the sum of all the port capacitance on the net

$Dc_{[s]}$ = interconnect timing delay of a given net segment, also referred to as the RC delay

Dc = Dc[1] + Dc[2]

where Dc[1] = interconnect delay for Metal 1

Dc[2] = interconnect delay for Metal 2

Dc[s] = Rwire[s] (Cwire[s] + Cinputport), where

Rwire[s] = resistance of the net segment from output to input port

Cwire[s] = capacitance of the net segment from output to input

Cinputport = load capacitance of the input port

4.9 Propagation Delay

4.9.2 Delay Calculations of Core Cell Nets (con't.)

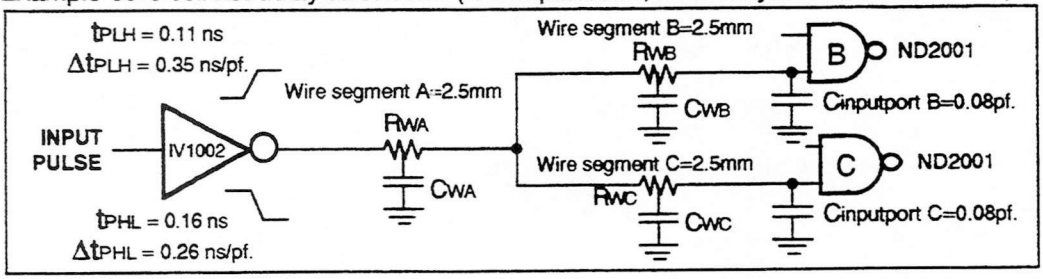
Here are the capacitance and resistance values per unit length of wire for the QYH500 Family :

Capacitance Metal 1 = 0.0001235 pf/μ Resistance Metal 1 = 0.0000566 KΩ/μ
Capacitance Metal 2 = 0.0000661 pf/μ Resistance Metal 2 = 0.0000228 KΩ/μ

Here is a chart showing some representative values per unit length of metal.

Metal Length		C in pf.		R in KΩ	
mm	μ	Metal 1	Metal 2	Metal 1	Metal 2
10.0	10,000	1.235	0.661	0.566	0.228
5.0	5,000	0.618	0.331	0.283	0.114
2.5	2,500	0.309	0.165	0.142	0.057
1.0	1,000	0.124	0.066	0.057	0.023
0.5	500	0.062	0.033	0.028	0.011

Example core cell net delay calculation (for simplification, all first layer metal is assumed) :



Di = tPLH = 0.11 ns. ΔtPLH = 0.35 ns/pf. Cinput B = Cinput C = 0.08 pf.
Di = tPHL = 0.16 ns. ΔtPHL = 0.26 ns/pf. Wire length C= 2.5 mm
Wire length A= 2.5 mm Wire length B= 2.5 mm

$$D_{t(LH)} = \Delta t_{PLH} \times (C_{wires} + C_{inputports})$$
$$= 0.35 \times [(C_{WA} + C_{WB} + C_{WC}) + (C_{inputportB} + C_{inputportC})]$$
$$= 0.35 \times [(0.309 + 0.309 + 0.309) + (0.08 + 0.08)]$$
$$= 0.35 \times 1.087 = 0.380 \text{ ns.}$$

$$D_{C[AB]} = R_{wire[AB]} \times (C_{wire[AB]} + C_{inputport})$$
$$= (0.142 + 0.142) \times [(0.309 + 0.309) + 0.08]$$
$$= 0.284 \times 0.626 = 0.178 \text{ ns.}$$

Therefore, $D_{[AB]} = D_i + D_t + D_{C[AB]}$
$= 0.11 + 0.380 + 0.178 = \mathbf{0.668\ ns.}$

4.9 Propagation Delay

4.9.3 Net Loading

The load capacitance on a given net is comprised of two factors;

$C_{inputports}$ = Input capacitance of each cell on the net

C_{wire} = The capacitance of the metal wiring of the net with the rest of the circuit

The sum of $C_{inputports}$ and C_{wire} must not exceed C_{MAX}. C_{MAX} is the value of C which results in rise and fall times becoming greater than 2ns in the QYH500 Family.

4.9.4 Estimated Net Load Capacitance

Before the chip is laid out, the wiring capacitance (Cw) and resistance (Rw) of each net is not known. In order to perform initial simulations, it is necessary to estimate the internal delays and therefore the capacitance and resistance of each net. This is done by employing "statistical capacitance", based upon designs of similar size.

After the chip is laid out, the exact capacitance and resistance values will be known, and will be "back-annotated" into the final, most accurate simulation.

4.9 Propagation Delay

4.9.5 Calculation of Output Pad Delay

The output response of a CMOS output macrocell is equivalent to the charge and discharge model of the load capacity. The delay time for the output is the sum of the cell internal delay and the load delay. The following are the equations for the delay time of an output cell :

$$t_{LH_{CLoad}} = t_{LH_{INT}} + (\Delta t_{PLH} \cdot C_{Load})$$

$$t_{HL_{CLoad}} = t_{HL_{INT}} + (\Delta t_{PHL} \cdot C_{Load})$$

where,
$t_{LH_{INT}}$ = Internal output cell delay, output going HIGH
$t_{HL_{INT}}$ = Internal output cell delay, output going LOW
Δt_{PLH} = HIGH drivability, in ns/pf
Δt_{PHL} = LOW drivability, in ns/pf
C_{Load} = Total output capacitance (input loads + wiring)

In the cell libraries, $t_{LH_{INT}}$, $t_{HL_{INT}}$, Δt_{PLH}, and Δt_{PHL} are not given for output cells, as they are for all the core macrocells. Instead, the following parameters are given, for 3 different capacitive loads :

t_{PZH} = nanoseconds delay (output going HIGH)
t_{PZL} = nanoseconds delay (output going LOW)

(Note: Although the symbols tPZH and tPZL usually refer to switching times from the high-impedance state, that is not the case here. In this case, Z refers to the output pad "Z").

Each of the above parameters are given for 3 different C_{Load} values (15pf, 50pf, and 100pf) for each output macrocell. For each C_{Load} value, minimum, typical and maximum nanosecond values are given.

If C_{Load} values different from 15, 50, or 100pf are required, use linear interpolation/ extrapolation to find the appropriate nanosecond delay time.

4.10 Special Cells

Array Structure

Chip Express arrays consist of rows of transistor pairs. The smallest repeating unit, called an array cell, consists of 4 transistors: 2 P-channel and 2 N-channel. For example, this unit can be used to build a 2-input NAND gate, which constitutes the gate unit used when counting the number of total "equivalent gates" available in the array. The rows of transistor pairs are separated by interconnect channels, where all possible connections are implemented. These connections are selectively erased by a laser-cutting process patented by Chip Express.

Hard Macrocells

The cell libraries consist of "hard-wired" cells which implement standard logic functions, such as 2-input NANDs, inverters, flip-flops, etc. These cells are considered "hard-wired" because their interconnect pattern is part of the cell data, and stays the same for every instance of the cell.

Soft Macrocells

Users can design their own cells, called "soft-macros". These macros are made up of hard-wired cells connected together. They are called "soft-macros" because the interconnect between the "hard-wired" cells is not fixed, and can vary from one instance to another.

Before place-and-route is executed, the soft macros are "flattened" down to their hard-cell components. There is no optimization or consistency of routing within a soft macro. Soft macrocells are merely a convenience for the designer to use a nesting feature.

Large Modules

Chip Express also offers "modules", which are larger functions using many gates, but where the placement and configuration is physically fixed. Such large macrocells include RAMs, dual-port RAMs, FIFOs, and DPLLs.

RAMs

The RAMs offered are synchronous, both single and dual-port. They range in size and organization from 4b x 4 Words to 32b x 256 Words. Refer to the tables for a list of read and write cycles for each RAM size. For more information on RAMs and FIFOs, please refer to the RAM application note in this book, or contact Chip Express.

FIFOs

The FIFOs offered are also for the QYH500 array family. They range in size and organization from 4b x 4 Words to 32b x 256 Words. Refer to the tables for a list of delays for each FIFO size. For more information on RAMs and FIFOs, please turn to the RAM/FIFO application note in this book.

DPLL

The DPLL macro is also available in the QYH500 array family. It is a digital DPLL which does not require any external components. Operating frequency ranges from 19 to 60MHz. The worst case phase error is 700ps (350ps typ.). Please turn to page 55.

4.11 The Digital Phase-Locked Loop (DPLL)

V1.1

1. Introduction

Most of today's synchronous designs use a clock driver or clock-tree distribution network to minimize the clock skew between flip-flops inside an IC. When a design contains more than one IC that has to communicate through a common synchronous bus, there is a problem synchronizing the internal clocks of the IC's. Even when all delays in each IC are known in advance, the variations in temperature, voltage and process between the ICs make this synchronization difficult to achieve.

In order to synchronize between clocks of different IC's, a DPLL is used. The DPLL's purpose is to eliminate the clock skew between different ICs, by adjusting the internal clock of each IC so that it is aligned with the external clock. This clock should be common to all the ICs in the design. The DPLL is built of a variable delay-line, long enough to store a whole period of the clock signal. The system clock is fed to this delay line, and then runs to the clock-tree distribution network. A sample clock from the output of this network is fed to the DPLL, which is constantly monitoring the phase difference between the system clock and the internal clock. When the phase difference exceeds the allowed limit, the delay of the delay-line is adjusted so that the internal clock will align with the system clock.

From the designer point of view, the QuICk DPLL is a "magical" black box. It cancels out the clock-tree distribution network's delay, at the price of a small initialization period (following RESET). The only change that has to be made in the design, in order to use the QuICk DPLL, is to pass the system clock through the DPLL, and to provide it with a sample of the clock-tree distribution network. Once initialization is complete, the QuICk DPLL will make sure that the system clock and the internal clock are aligned, even if internal delays inside the IC change (e.g., as a result of a change in temperature).

2. Specifications

Operation frequency :	19MHz. - 60MHz.
Phase Error :	700 ps (worst)
	350 ps (typical)
Initialization Time :	0.063 msec maximum (1100 clocks)
Availability :	All QYH500 members

4.11 The Digital Phase-Locked Loop

3. Structure of the QuICk DPLL

The QuICk DPLL is composed of 3 main components :

- Phase detector
- Counter
- Variable delay-line

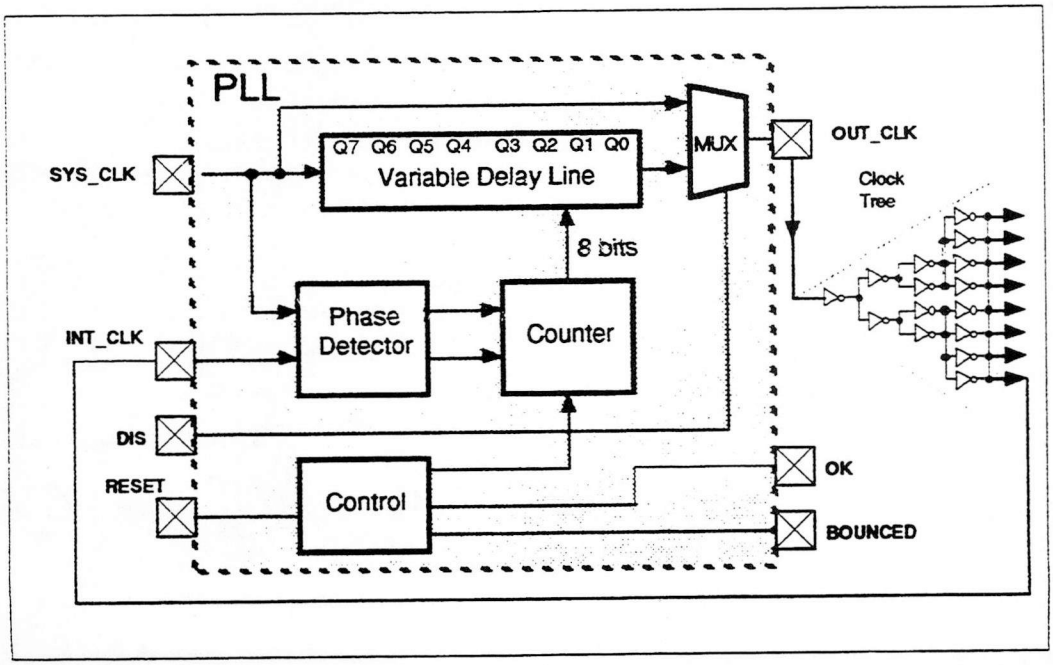
The phase detector compares the system clock with the internal clock, providing information about the relative phase of the internal clock vs. the system clock. This information is used by the counter, as it tries to reduce the phase error.

The counter supplies the delay line with a word that selects the delay value. Based on the information supplied by the phase detector, it increases/ decreases this value, or leaves it unchanged. The counter operates at 1/4 of the system clock frequency, making a correction every 4 system clock cycles.

The delay-line creates a variable delay from the system clock (input) to the output clock, according to the delay word supplied by the counter.

In addition, a MUX at the output of the delay-line permits the disabling of the DPLL for testing purposes.

DPLL Block Diagram



4.11 The Digital Phase-Locked Loop

4. Using the QuICk DPLL

The QuICk DPLL is a soft macro called **pll_16_60**. In addition to the necessary clock connections, more input/output signals are provided to enhance testability. The following is a list of all the QuICk DPLL I/O signals and their descriptions :

Signal Name	Signal Type	Function
SYS_CLK	Input	System clock. Reference signal for the DPLL. There is no limit on the duty cycle of SYS_CLK, as long as the high and low periods are at least 2nsec each.
IN_CLK	Input	Internal clock. Sample from the output of the clock-tree distribution network. The QuICk DPLL makes sure this signal's falling edge is aligned with the falling edge of SYS_CLK.
DIS	Input	Disable. When '0', the DPLL operates normally. When '1', SYS_CLK is passed directly to OUT_CLK, without going through the delay line.
RESET	Input	DPLL Reset. When '1', the DPLL operates normally, When '0', the tracking mechanism of the DPLL is disabled, the delay line is set to the smallest delay possible, and Q7-Q0 are 0.
OUT_CLK	Output	Clock output. This clock goes to the input of the clock-tree distribution network.
BOUNCED	Output	Provides information about the internal status of the DPLL. A '0' indicates the normal condition. A '1' signals that the DPLL is still in the process of initialization. BOUNCED=0 does NOT mean the system and internal clocks are aligned.
OK	Output	'1' means that the internal clock is aligned with the system clock, and the DPLL is stable. '0' indicates that, during the last falling edge of SYS_CLK, the phase error between SYS_CLK and INT_CLK exceeded the allowed limit.
Q7 - Q0	Output	The internal state of the delay line (Q7=MSB).

Notes :
After power-on, the DPLL may take up to 1100 system clocks for initialization, prior to stabilization. Although RESETting the DPLL after power-on is not mandatory in the actual circuit, for simulation purposes it is necessary to activate RESET for at least one clock period, so that all the internal registers will come to a known state.

4.11 The Digital Phase-Locked Loop

Following the positive edge of RESET, the counter outputs Q7-Q0 will be 0, and start counting up at 1/4 of the system clock rate. At this time, BOUNCED can be in any state, and OK is 0. Once alignment of INT_CLK with SYS_CLK is achieved, OK gets set to 1, and BOUNCED is set to 0. With time, as the internal delays inside the IC drift (due to temp. change, etc.), the PLL detects the phase error, and corrects it. During a phase-error period, OK might get set to 0 for a period of a few clocks, until the delay line adjusts to correct the phase error.

During normal operation, BOUNCED is 0, and OK is 1. Sometimes, when the phase alignment is marginal (due to the delay drift), OK might toggle between 1 and 0 for a long time, before a correction is made by the DPLL — this is normal. The OK line is updated at every falling edge of SYS_CLK. An error situation can be detected by monitoring the OK line, looking for a series of 12 '0's in a row (the OK line can be sampled at every rising edge of SYS_CLK. This means that the DPLL has made at least 2 delay-line corrections, and the clocks are still not aligned. Since the phase drift should be very slow under normal conditions, 1 delay-line correction should suffice to restore phase alignment at any time, so 12 '0's in a row indicate a problem.

The DIS input signal can be used to isolate the DPLL from the rest of the IC, and is also used for testing purposes. When DIS=1 and RES=1, the DPLL is still active and tries to align INT_CLK with SYS_CLK. However, because the feed-back loop is not active, and the delay line has no effect, the phase detector will always measure the same phase error. This will result in the counter counting from 00 to FF, and then back to 00 (bouncing between the 00 and FF walls). The count will increment/ decrement every 4 system clocks, as usual.

During simulation, it is important to provide at least 1100 test vectors at the beginning of the simulation, during which the DPLL will have time to stabilize. During that time, the internal clock inside the IC is not aligned with the system clock, and therefore, functions that depend on this alignment cannot be tested during the first 1100 test vectors. The first few vectors should contain RESET=0 to start the DPLL counter from a known value. Following those 1100 vectors, the simulation can proceed as usual, with the DPLL being transparent to the rest of the design.

4.12 RAM Implementation (ver. 12-94)

Scope

This document describes the features and operation of the Static RAM, designed for the QYH500 family of Gate-Arrays from Chip Express. There are three configurations of RAM possible. These are :

- Single Port RAM
- Dual-Port RAM
- FIFO RAM

Features

- Fully Static Operation
- Low Stand-By Power
- Synchronous Operation
- Number of Bits from 1 to 64
- Full Parallel Access with separate input and output ports
- Address Range from 2 to 1,024 words (addr. lines from 1-10)

Description

Throughout this document :

- M is the number of RAM words
- N is the number of RAM bits
- m is the number of address lines
- Always : $2^m >= M > 2^{m-1}$

The RAM has 2 phases of operation. In the first phase, the **clk_ram** input is high, determining a precharge. In the second phase, the clock input is LOW, determining the actual Read or Write operations. The WE input signal determines the type of operation in the second phase. When WE is HIGH, writing is enabled; when WE is LOW, reading is enabled.

The address lines **add_ram**[(m-1):0] determine the address of the operation. The falling edge of the **clk_ram** signal latches the **add_ram** lines.

The data lines on the output are latched on the rising edge of the **clk_ram** signal. Therefore, data from a current RAM cycle will be stable on the outputs until the following falling edge of the **clk_ram** signal.

In a WRITE operation, data asserted on the **data_ram**[(N-1):0] lines, meeting the specified set-up times, will be written. This data will also appear on the **q_ram** lines.

In a READ operation, data will appear on the **q_ram** lines, at a specified amount of time after the second phase begins.

The **clk_ram** signal is used to perform the pre-charge, the address and output data latch only. It is not used in any way to refresh the memory. This signal can be stopped at any time without a loss of memory. If conservation of power is required, it is best to keep the **clk_ram** signal at the HIGH state. This way, the sense amplifiers, which consume a lot of power, are off.

In a dual-port RAM, there are 2 independent ports for accessing the RAM; Port A and Port B. These include :

two sets of address lines:	**add_ram_a,**	**add_ram_b**
two sets of data input :	**data_ram_a,**	**data_ram_b**
two sets of data output :	**q_ram_a,**	**q_ram_b**

4.12 RAM Implementation

Description (con't.)

Each of the sets is associated with the appropriate WRITE signal, **we_ram** and **we_ram_b**. During the same cycle, it is not allowed to perform a WRITE/WRITE, a WRITE/READ , or a READ/WRITE operation from ports A and B, to the same address location.

In the FIFO RAM, there are 2 independent ports for accessing the RAM : A and B. Port A is used for WRITE operations. Port B is used for READ operations. These include :

two sets of address lines: **add_ram_a, add_ram_b**
data input for Port A: **data_ram**
data output for Port B : **q_ram**

Port A is associated with the WRITE signal **we_ram_a**. During the same cycle, it is not allowed to access the same address location from both ports.

Signal Name	Function Name	Edge/ Level	Description
clk_ram	Clock	↓ 1	Read or Write Precharge
we	Write Enable	0 1	Read Write
add_ram	RAM Address	↓	RAM address is latched on falling edge of clock.
data_ram	Data In	↑ ↓	Data In is latched on rising edge of clock, or falling edge of we.
q_ram	Data Out	↑	Data Out is latched on the rising edge of clock.

Dual-Port RAM Signals

Signal Name	Function Name	Edge/ Level	Description
clk_ram	Clock	↓ 1	Read or Write Precharge
we_ram_a	Write Enab. Port A	0 1	Read Port A Write Port A
add_ram_a	Address In Port A	↓	Latch Port A address on falling edge of clock
data_ram_a	Data In Port A	↑ ↓	Latch Port A data on rising edge of clock, or or falling edge of we.
q_ram_a	Data Out A	↑	Port A output data is latched on the rising edge of clock.
we_ram_b	Write Enab. Port B	0 1	Read Port B Write Port B
add_ram_a	Address In Port B	↓	Latch Port B address on the falling edge of clock.
data_ram_b	Data In Port B	↑ ↓	Latch Port B data on the rising edge of clock, or the falling edge of we.
q_ram_b	Data Out B	↑	Port B output data latched on the rising edge of clock.

4.12 RAM Implementation

FIFO RAM Signals

- Port A is the WRITE port
- Port B is the READ port

FIFO RAM Signals

Signal Name	Function Name	Edge/ Level	Description
clk_ram	Clock	↓ 1	Read or Write Precharge
we_ram_a	Write Enab. Port A	0 1	Read Port A Write Port A
add_ram_a	Address In Port A	↓	Latch Port A address on the falling edge of clock.
data_ram	Data In Port A	↑ ↓	Latch Port A data on the rising edge of clock, or the falling edge of we.
add_ram_b	Address In Port B	↓	Latch Port B address on the falling edge of clock.
q_ram	Data Out Port B	↑	Port B output data is latched on the rising edge of clock.

RAM Sizes

Possible Number of Words

The RAM implementation is divided into blocks of RAM (RAM rows). The number of blocks depends on the number of words of the RAM. These blocks also dictate possible RAM sizes. In small RAM implementations, a single block is used, but since RAM bits are implemented in pairs, only even numbers of addresses can be implemented. It is always possible to use a RAM with numbers of words not as specified below, although the actual implementation will be as specified in the table below.

Number of Words	Step
2 - 32	2
36 - 64	4
72 - 128	8
144 - 256	16

4.12 RAM Implementation

RAM Sizes

The following is a list of example RAM sizes for the 3 types of RAMs offered. The numbers in parentheses represent the gates-per-bit ratio. For a RAM size different than those shown, please consult with Chip Express.

Single-Port RAMs - Gates Required (gates/bit)

	Bits			
Words	4	8	16	32
4	181 (11.3)	297 (9.3)	535 (8.3)	1,019 (7.9)
8	252 (7.8)	400 (6.2)	702 (5.4)	1,322 (5.1)
16	382 (5.9)	594 (4.6)	1,024 (4.0)	1,416 (3.7)
32	630 (4.9)	970 (3.7)	1,656 (3.2)	3,092 (3.0)
64	915 (3.5)	1,531 (3.0)	2,834 (2.7)	5,440 (2.6)
128	1,481 (2.8)	2,713 (2.6)	5,190 (2.5)	10,144 (2.4)
256	2,665 (2.6)	5,065 (2.4)	9,886 (2.4)	19,528 (2.3)

Dual-Port RAMs - Gates Required (gates/bit)

	Bits			
Words	4	8	16	32
4	335 (21)	551 (17)	992 (15)	1,890 (14)
8	461 (14)	725 (11.3)	1,262 (9.8)	2,368 (9.2)
16	689 (10)	1,049 (8.2)	1,778 (7.0)	3,300 (6.4)
32	1,121 (8.7)	1,673 (6.5)	2,768 (5.4)	5,140 (5.0)
64	1,563 (6.1)	2,539 (4.9)	4,630 (4.5)	8,812 (4.3)
128	2,439 (4.8)	4,391 (4.3)	8,318 (4.1)	16,172 (3.9)
256	4,295 (4.2)	8,071 (3.9)	15,662 (3.8)	30,844 (3.8)

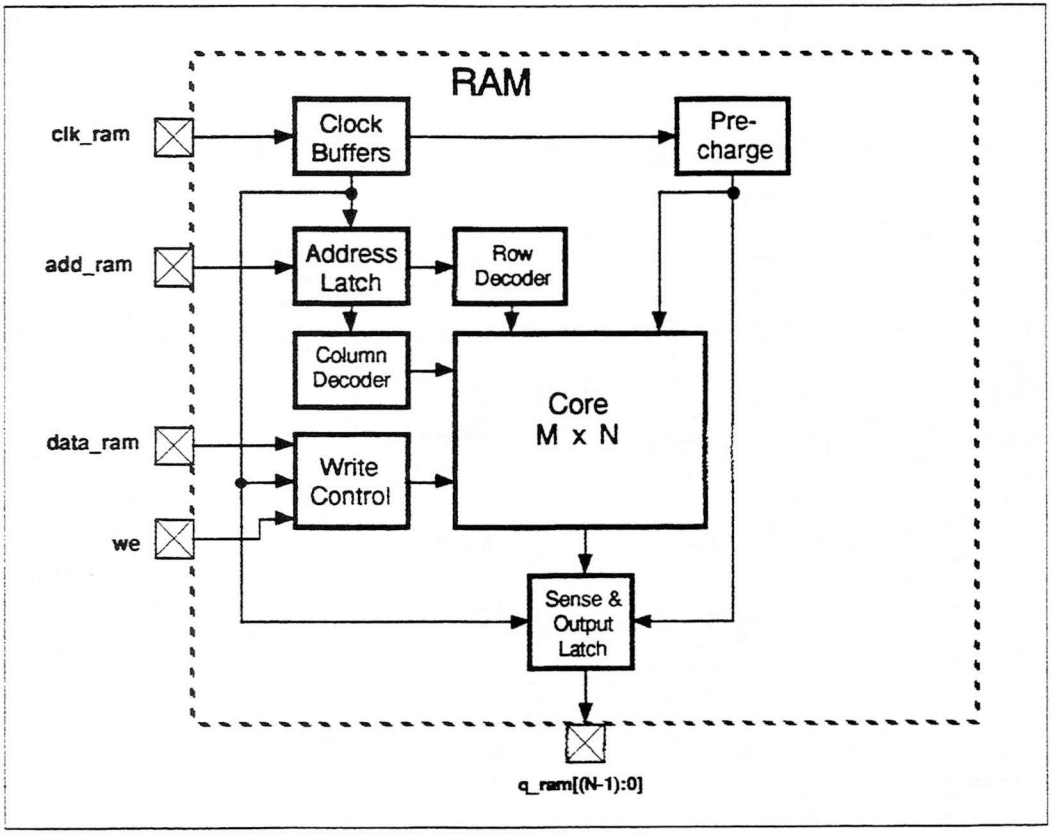
FIFO RAMs - Gates Required (gates/bit)

	Bits			
Words	4	8	16	32
4	269 (16.8)	421 (13.1)	732 (11.4)	1,370 (10.7)
8	395 (12.3)	595 (9.3)	1,002 (7.8)	1,848 (7.2)
16	623 (9.7)	919 (7.1)	1,518 (5.9)	2,780 (5.4)
32	1,055 (8.2)	1,543 (6.0)	2,526 (4.9)	4,620 (4.5)
64	1,497 (5.8)	2,409 (4.7)	4,370 (4.2)	8,292 (4.0)
128	2,373 (4.6)	4,261 (4.1)	8,058 (3.9)	15,652 (3.8)
256	4,229 (4.1)	7,941 (3.6)	15,640 (3.7)	30,324 (3.7)

4.12 RAM Implementation

RAM Block Diagrams

Single-Port RAM Block Diagram



The address is latched in the Address Latch on the falling edge of the clock. One part of the address is used to decode the address within the block (Row Decoder). The other part is used to select the block (Column Decoded).

The pre-charge circuitry is used to pre-charge the core cells, as well as the Sense Amplifiers on the output.

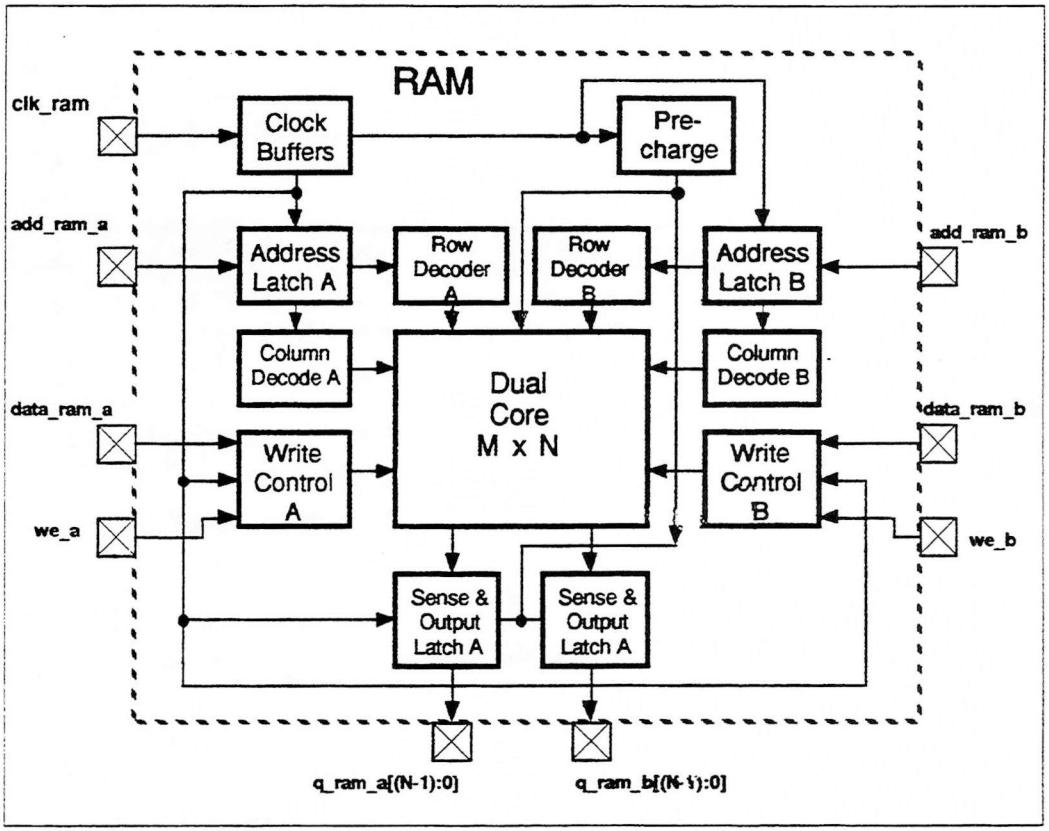
The input data is written through the Write Control logic during a WRITE cycle.

The data on the output is latched when the clock is HIGH. This is true for both the Read and the Write cycles.

4.12 RAM Implementation

RAM Block Diagrams (con't.)

Dual-Port RAM Block Diagram

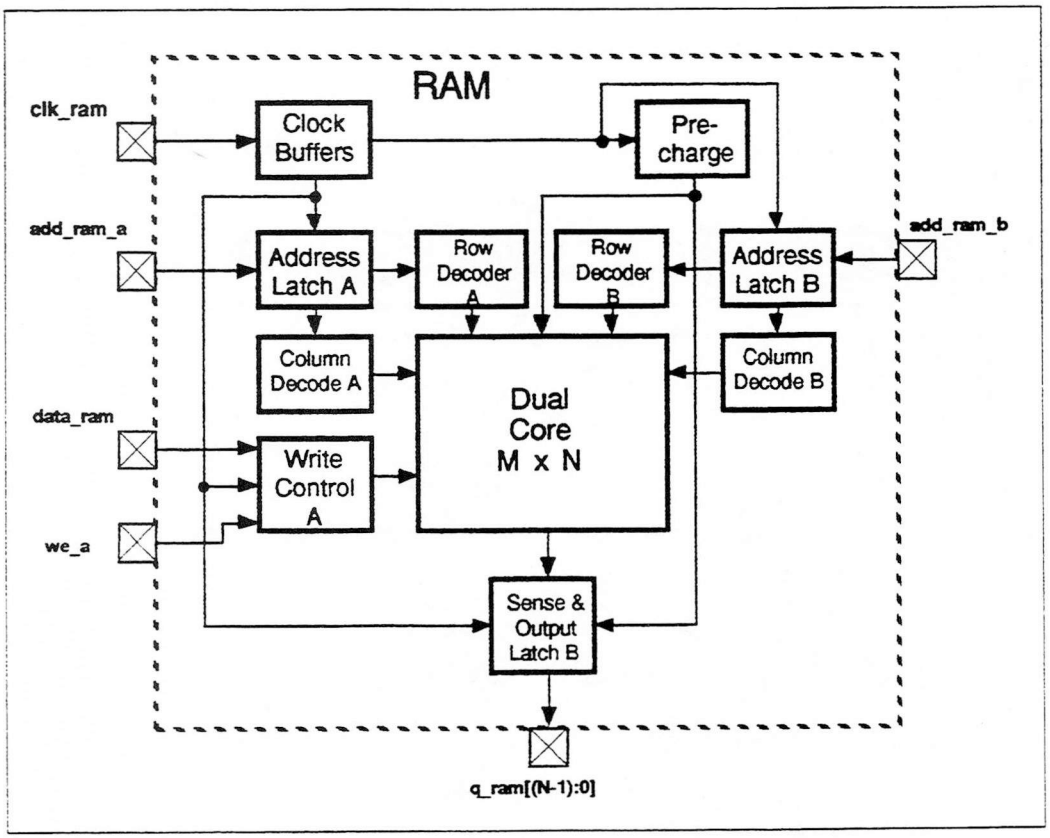


The operation of the Dual-Port RAM is the same as the Single-Port RAM. The only difference is that the Dual-Port RAM has two independent sets of addressing and data that access the same RAM. The only restriction is that, during the same cycle, it is not allowed to access the same address from both ports.

4.12 RAM Implementation

RAM Block Diagrams (con't.)

FIFO RAM Block Diagram



FIFO RAM has 2 separate addressing mechanisms. Port A is used only for Write operations. Port B is used only for Read operations.

4.12 RAM Tools Integration

The RAMs are fully integrated into the QuICk™ software. The process of generating the RAM is fully automatic. The RAM modules are typically generated by the application engineers at Chip Express. The output is sent to the customer. The data sent typically includes a high-level description of a desired RAM module, for those who are using a Verilog environment. For back-annotation purposes, a low-level model of the RAM in Verilog or Synopsis format is available.

Verilog High-Level

The Verilog high-level model supplied is for every RAM module. There can be several RAM modules in each design. For each RAM used, a file having the description for that specific RAM will be supplied. The example below shows the first part of such a file. The file is an example of a single-port RAM with 40 words and 2 bits.

```
/************************************************/
/*      RAM BLOCK: 40 WORDS, 2 BITS             */
/************************************************/

/************************************************/
/*      THE CALL FOR THE RAM                    */
/************************************************/
/*ram1 ram1_inst ( add_ram(0), add_ram(1), add_ram[2], add_ram[3], add_ram[4] , add_ram[5]
        data_ram[0], data_ram[1]
        q_ram[0], q_ram[1], we_ram, clk_ram)*/
/************************************************/
/*      THE RAM MODULE :                        */
/************************************************/
'timescale 1ns / 10ps
module ram1 ( add_ram(0), add_ram(1), add_ram[2], add_ram[3], add_ram[4], add_ram [5]
        data_ram[0], data_ram[1]
        q_ram[0], q_ram[1], we_ram, clk_ram) ;
parameter SIZE=2  ;
parameter LEN=6  ;
parameter LEN_BLOCK=6  ;
parameter NUM_OF_BLOCKS=2  ;
input [LEN-1 : 0] add_ram
input [SIZE-1 : 0] data_ram
input  we_ram, clk_ram ;
output [SIZE-1 : 0] q_ram ;

wire  [LEN_BLOCK-1 : 0] add_blk ;
wire  [NUM_OF_BLOCK-1 : 0] sel_blk
...
```

The file should be included as an additional file for the Verilog simulation. Under the section titled : "The Call For The RAM", appears a commented Verilog module call. This whole statement should be copied, uncommented, to the appropriate place in the design, where the RAM is instantiated.

4.12 RAM Implementation

Verilog High-Level (con't.)

This statement will do the link between the supplied RAM module and the actual design. This process should be repeated for each RAM module in the design.

Note: This RAM module is used for simulation only. If a synthesis tool such as Synopsys is used, it should not be used to synthesize the RAM module. The RAM synthesis is done only by the internal QuICk RAM compiler tool.

In back-annotation, the RAM appears as a flat netlist as part of the whole flat design. This is true for both Verilog and Synopsys environments.

RAM Timing

Since RAM timing depends on the actual size of the RAM, the RAM timing is supplied on a per-RAM basis. Please contact Chip Express for more information on the RAM.

Specification Example- 32 x 8 RAM

Read Cycle

Symbol	Parameter	Best	Typical	Worst	Unit
t CKR	CIK period (min)	7.08	10.72	17.91	ns
t HCK	CLK HIGH (min)	0.51	0.77	1.29	ns
t LCKR	CLK LOW (min)	6.57	9.95	16.62	ns
t ASU	Address set-up (min)	0.00	0.00	0.01	ns
t AH	Address hold (min)	0.63	0.95	1.59	ns
t QV	Old output valid (min)	0.62	0.94	1.57	ns
t PCQR	Clock to valid data (max)	7.17	10.87	18.15	ns
t WH	WE hold after Clock (min)	0.80	1.21	2.02	ns
t WSF	we_ram set-up to Clock	0.00	0.00	0.00	ns

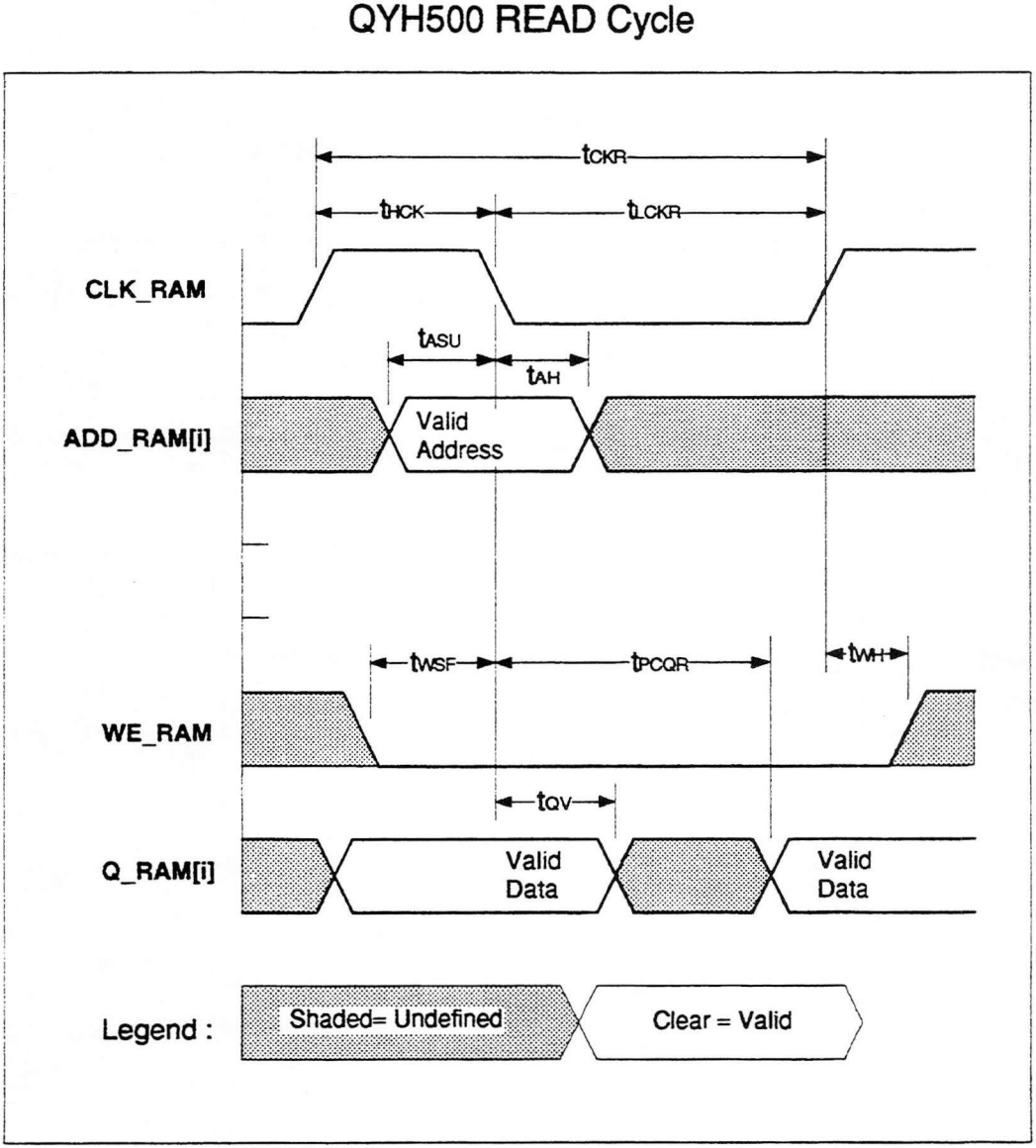
WRITE Cycle

Symbol	Parameter	Best	Typical	Worst	Unit
t CKW	CIK period (min)	5.62	8.52	14.23	ns
t HCK	CLK HIGH (min)	0.51	0.77	1.29	ns
t LCKW	CLK LOW to valid write(min)	5.11	7.75	12.94	ns
t ASU	Address set-up (min)	0.00	0.00	0.01	ns
t AH	Address hold (min)	0.63	0.95	1.59	ns
t DSU	Data set-up (min)	1.85	2.81	4.68	ns
t DH	Data hold (min)	0.39	0.59	0.99	ns
t HW	we_ram HIGH (min)	3.51	5.31	8.87	ns
t QV	Old output valid (min)	0.62	0.94	1.57	ns
t PDQW	Valid data to output (max)	2.08	3.15	5.26	ns
t DSC	Data set-up to Clock (min)	2.24	3.40	5.68	ns
t DHC	Data hold after Clock (min)	0.00	0.00	0.00	ns
t WHC	WE hold after Clock (min)	0.00	0.00	0.00	ns

Note : tPDQW is valid only when the WE input is kept HIGH, while valid DATA is input.

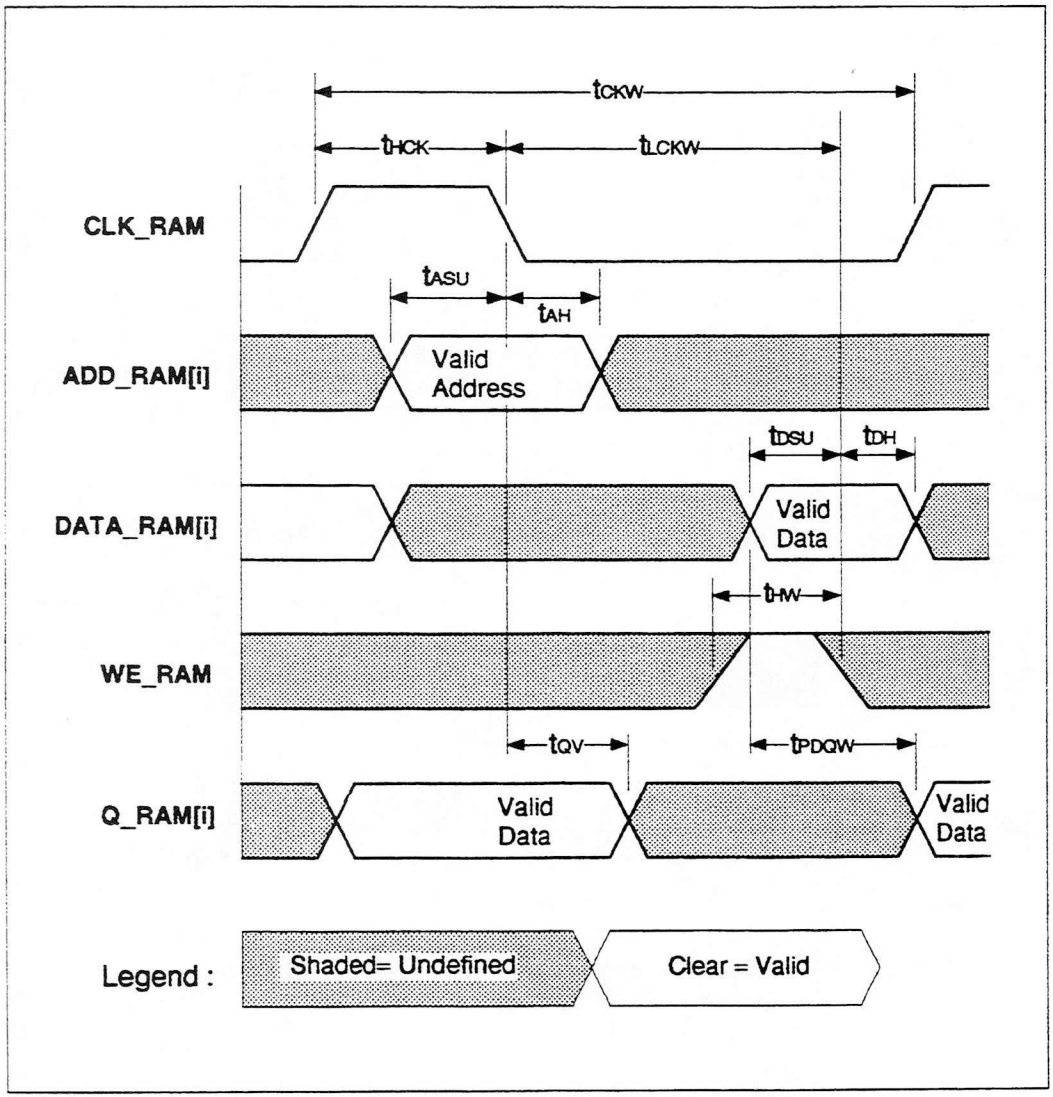
4.12 RAM Implementation

QuICk Clocked RAM



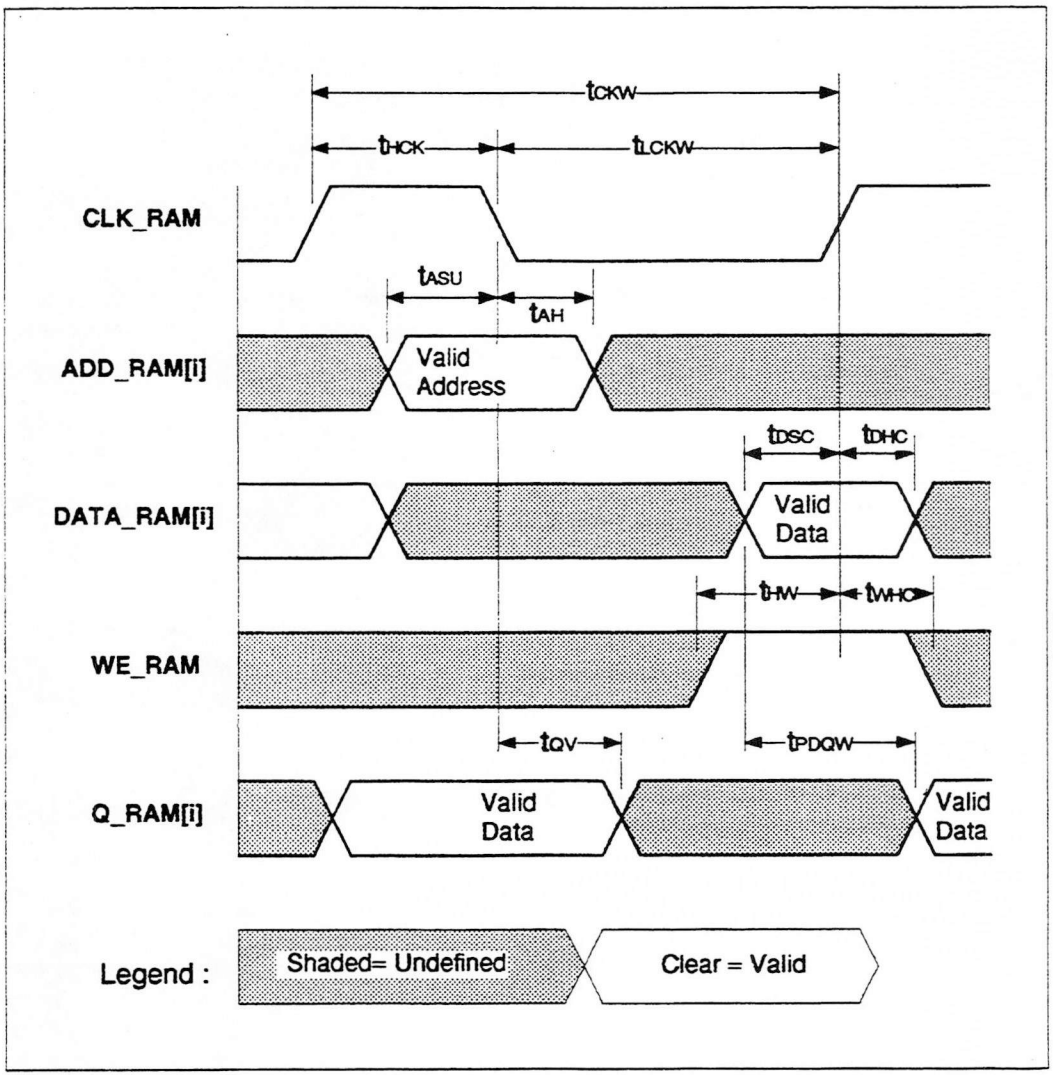
4.12 RAM Implementation

QuICk Clocked RAM



4.12 RAM Implementation

QuICk Clocked RAM



4.13 Testability

A design which is not testable is not economically manufacturable. The ability to test the circuit should be part of the design process. Test time should be as quick and efficient as possible to reduce costs.

In general, in order to achieve an elegant, complete and fast test implementation, Chip Express recommends the following :

Initialization :

Include a full-chip reset in the design. It increases node visibility, and facilitates test vector generation. A chip that cannot be initialized cannot be tested.

Synchronous circuits :

Design fully synchronous circuitry. Avoid built-in race conditions, clock-gating, edge-detector type one-shots, etc. These techniques are process sensitive and are likely to cause failures if process parameters change.

Active Busses :

Ensure that busses are always driven and do not have any high impedance states. These states generate noise into the circuit and cause parasitic power consumption. They also prevent I_{DDQ} testing.

Special Test Modes :

Add separate test modes for embedded RAMs and FIFOs. Provide a separate test input that reallocates pinout, and allows direct access to the RAM or FIFO. This feature will greatly reduce test time and manufacturing cost with it.

Incorporate Test Structures :

Boundary Scan :

Add boundary scan logic into the design. This does not cost much extra logic, and greatly reduces the number of test vectors required, if the tester will support it.

Multiplexed I/Os for Large Block Testing :

This technique allows isolation of every major block in the design, so that they can be tested independently from the rest of the chip.

Built-in Self-Test (BIST) :

Well-suited for RAMs, this 3-wire technique tests a partition of the logic by using internally-generated vectors.

IDDQ Testing :

Maximize test efficiency by using IDDQ testing. This method of testing CMOS circuits is very efficient at finding faults early-on in the test sequence, and does not require many test vectors. I_{DDQ} testing consists of measuring the I_{DD} current for various input logic combinations. Many logic faults occur because there is a parasitic current path somewhere in the circuit. Any open wire can produce a floating input. In CMOS, that means oscillations and high current consumption in the gates involved. Conversely, a short circuit between two wires will result in current flow if each wire is driven to opposite logic levels.

4.14 Fault Coverage

Controllability - The ability to set to "1" or "0" internal nodes in the design from the input pins.

Observability - The ability to observe at the output pins "stuck-at" fault situations of internal nodes in such a way that will change expected output results.

In each design, there will probably be a number of internal nodes that faults can neither be controlled nor can be observed. These are untestable nodes.

Fault coverage is the ratio between the number of detected faults, and the number of all possible faults.

$$\text{Fault coverage} = \frac{\text{\# of detected faults}}{\text{\# of possible faults}} \times 100$$

The test program should be run through a fault simulator to verify fault coverage. Most logic simulators and hardware accelerators will provide that information, along with simulation results.

Chip Express does not require minimum fault coverage for laser parts, but requires 95% coverage for mass production parts (unless the customer signs a waiver). If the fault coverage for production parts is below 95%, additional test vectors need to be generated. Chip Express has software available to do ATPG (Automatic Test Program Generation).

4.15 ATPG

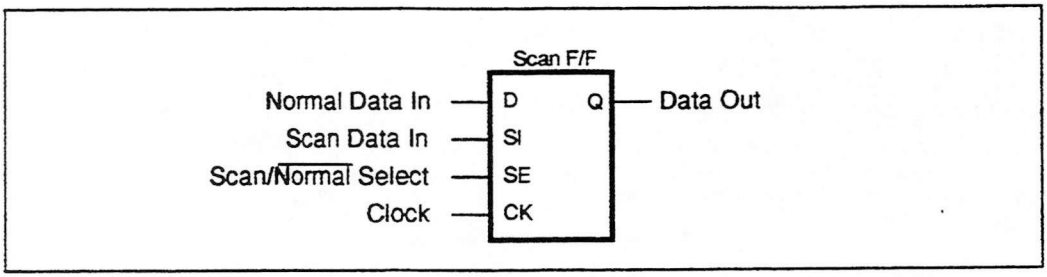
ATPG reduces dramatically the labor needed to develop test patterns that will achieve high test coverage. The ATPG combines both hardware changes (i.e., changes to the original design) and software that develops the vectors.

Chip Express currently supports an Automatic Test Program Generation Tool.

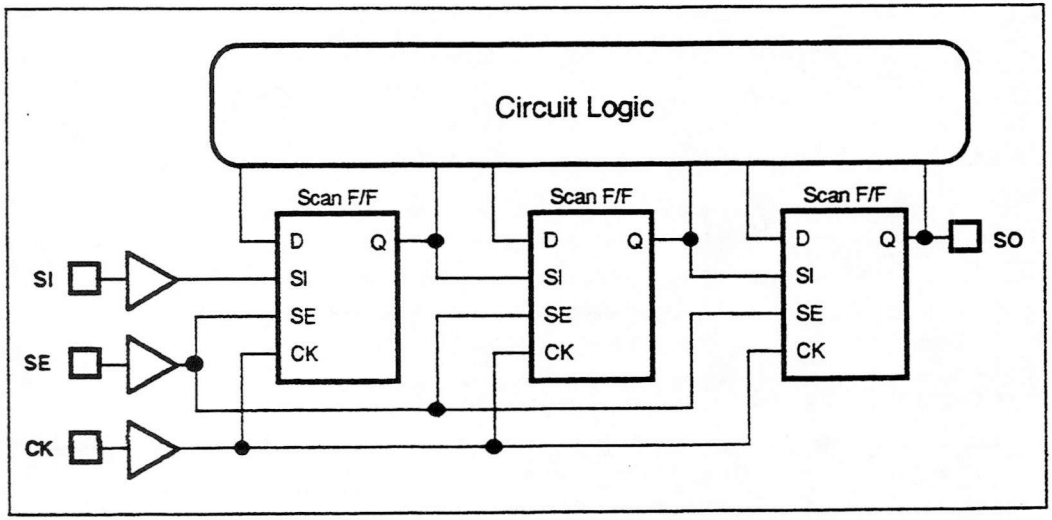
In ATPG, all sequential elements are connected to form a shift register or a scan-chain (this is called full scan). To the ATPG process, at least 3 I/O pins are devoted, 2 inputs and 1 output. The inputs are *scan mode/normal operation select* and SR input. The output is SR output. In some configurations, an additional clock input may be needed.

4.15 ATPG (con't.)

Each flip-flop in the design is turned into a muxed flip-flop (scan F/F).



Next, all the scan flip-flops are connected in a chain (shift register) configuration.



All vectors are inserted through SI and are read through SO. The SE enables the operation. The process involves insertion of a serial vector (while reading the previous vector) through the chain. Then SE changes state to normal operation, a clock is inserted, again switching to scan mode, reading the results while inserting the next vector.

Through scan and ATPG, high test coverage can be achieved.

4.16 Optimizing the Design

The circuit design should be carefully examined to reduce pin count, improve speed, testability, reliability, and reduce gate count. Here is a summary of techniques for optimizing design. Trade-offs of these techniques should be considered during the logic design phase.

Pin Count

Much of the total cost of a circuit is in the package; reduce the pin count as low as possible. Pin count may be reduced by the following methods :

- Test pins may be reduced by decoding input patterns which never occur in the circuit's normal operation.
- Transfer data in serially, not in parallel, whenever possible.
- Multiplex data busses and address busses, to match data and address bus multiplexing in most microprocessor designs.
- Use data latches to allow high- and low-order data to be multiplexed.

Speed — To improve the speed of a circuit, consider the following :

- Use a carry look-ahead/ carry propagate approach when designing counters or fast adders.
- Use power (high-drive) gates for high fanout outputs.
- Use NAND gates instead of NOR gates whenever possible.
- Always use available macrocells and avoid building logic from discrete gates (for example, do not build latches from NAND gate macrocells).
- Use AND-OR-INVERT elements when fanout is low.
- Separate the critical path by duplicating logic in a signal path.
- Locally buffer a signal driving a heavy load, such as a clock line.

Testability — There are also several methods for increasing testability :

- Use circuits that have a reset function, so that they can be externally initialized.
- Add logic that can be externally controlled in a system, using serial multi-stage connections of shift registers and counters.
- Design a system for which internal logic conditions can be set and detected by adding a test circuit with external test signals and clock signals.
- Set up an external test control signal in addition to an internal signal, if a long interval results from a clock input that is generated internally.
- Multiplex normal inputs and outputs with test control pins.

Reliability

- Use the recommended fixed-power-pin pinout for the chosen package; this ensures low-noise switching.
- Employ slew-rate controlled output buffers to reduce noise.

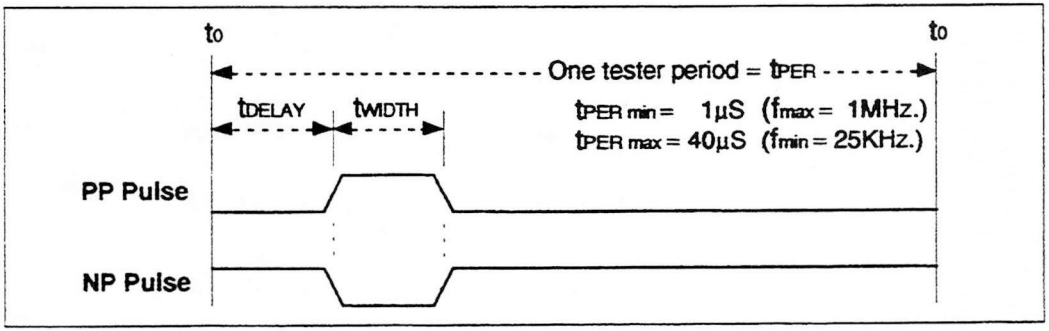
5.1 Signal Timing

In simulation, there is a great deal of freedom with regard to edge timings. However, the tester requires a well-defined set of timings in order to achieve accurate results. An engineer wants to be sure to measure the device, and not measure the tester. Therefore, the following conventions and guidelines are used.

5.2 Tester Considerations

Test signal nomenclature :

Input signals : 0 = Force LOW
1 = Force HIGH
Z = Tri-state
Two types of input pulse, with programmable delay and width :



Output signals : x = Don't care
L = Output is LOW
H = Output is HIGH

Tester Specifications :

# of input signal generators	=	12	max.
# of output strobe generators	=	4	max.
Min. spacing between input signal generators	=	100	ns.
Worst case skew between input pins	=	5	ns. pin-to-pin
Minimum tester period	=	1	µs.
Maximum tester period	=	40	µs.
Minimum tester clock speed	=	25	KHz.
Maximum tester clock speed	=	1	MHz.

5.3 Test Vector Guidelines

To enable the tester to handle signals according to the test file header specifications, and to verify the design according to user requirements, the following rules are used :

EXTERNAL SIGNALS :

- Each external signal should be connected to a QuICk™ hard I/O macrocell; external input signals to hard macro inputs, external output signals to hard macro outputs, and bi-directional signals to bi-directional hard macros.

5.3 Test Vector Guidelines

EXTERNAL SIGNALS (con't.)

- Place the I/O signals on the top level module of the design.
- 0, 1, X, and Z are the only legal forcing values.
- The minimum gap between timing generators should be 100ns.
- The user should verify that the test vectors reflect the behavior of the finished gate-level design. It is recommended to verify that the test vectors are correct, while running the design with best case, nominal, and worst case environmental and process conditions.
- Never force the values of internal signals during the simulation.

INITIALIZATION

- It is strongly recommended to design the circuit so that it can be initialized to a known state within the first few test vectors.
- Begin your simulation with vectors that initialize the circuit.

CLOCK SIGNALS

- Each clock signal is considered as 2 input signals (timing generators).
- Each clock input must be assigned to a "non-active" value in the first test vector.
- If a clock signal should not be active in the pattern, then it's value should be "0" for a positive clock (PP), and "1" for a negative clock (NP).

BI-DIRECTIONAL SIGNALS

- Each bi-directional signal is considered as 1 input and 1 output (tim.gen.).
- A bi-directional signal must be in one definite mode during a cycle. It can be in "input mode" or in "output mode". Split-cycle is not supported.
- Do not apply input data to a bi-directional signal when it changes its mode from input to output.
- No input data is to be applied to a bi-directional signal when in output mode. When a bi-directional signal is in output mode, it is handled as an output signal.

OUTPUT SIGNALS

- Output data is ignored for a bi-directional signal in an input mode. When a bi-directional signal is in input mode, it is handled as an input signal.
- The tester cannot check tri-state values. When the strobed value of an output or bi-directional signal is tri-state, the signal value in the test vector word is set to "X".
- Pull-up or pull-down values require special tests in the tester. Therefore, pull-up or pull-down output values should not be checked by the generated utility. When the strobed value of an output signal is pull-up or pull-down, the signal value in the test vector output word is set to "X".
- Do not submit simulation vectors if there is any timing violation error.
- Do not submit simulation vectors if there is any contention error.
- The minimum tester period should be 1µs. (1MHz. = fmax.)

5.4 CTV (Chip Express Test Vectors)

Chip Express requires the test vectors be given in a standardized format, called CTV. The CTV file contains 3 sections:

1. **Comment section**
2. **Timing section**
3. **Signal and Vector section**

1. Comment Section

This section should be used to define the design name, package type, date, etc. The common section begins with the word @COMMON, and ends with the word @ENDCOM. Each statement in this section starts with the character $. Anything can be written inside this section, since it is a comment section only, and is ignored.

Conventions:
Each CTV statement is written on one line. To continue a statement to the next line, the + character must be the first character of the next line.

All comments in the CTV file are specified by the character $. Anything from the $ to the end of the line is a comment, and is ignored.

Signal names in the CTV file are defined in 2 forms, simple names and names enclosed by single quotation marks.

2. Timing Section

This section describes the cycle time of the testing, each input stimulus time, each output strobe time, and the delay and width of each clock. The timing section begins with the word @TIMING, and ends with the word @ENDTIME. All the timing values should be given in nanoseconds, and should be integer numbers. All timing numbers are based upon the beginning of the cycle, to.
Signals that have the same timing specifications, can share the same timing statement.

Inside the timing section, the following statements may be used:

CYCLE <cycle number>

This statement defines the cycle length during testing, in ns.
This statement must be in the timing section.
Only one CYCLE statement is allowed.

INTIM DT=<time>
<list of signals>

The INTIM DT statement defines the time when the input signal will change to the value specified in the vector, in ns.
The <list of signals> statement is a list of all the input signals that have the <time> stimulus time.

5.4 CTV

2. Timing Section (con't.)

INTIM PP=<rise>,<fall>[<rise>,<fall>]
<list of signals>

The INTIM PP statement defines the time for positive clock signals. The <rise> defines the time in ns when a clock signal changes its value from a 0 to a 1. The <fall> defines the time when a clock signal changes its value from a 1 to a 0. The statement may contain more than one <rise> and <fall> command, which defines a "multi-pulse" positive clock. The <list of signals> statement is a list of all the positive clock signals that have the above timing specifications.

INTIM NP=<fall>,<rise>[<fall>,<rise>]
<list of signals>

The INTIM NP statement defines the time for negative clock signals. The <fall> defines the time in ns when a clock signal changes its value
from a 1 to a 0. The <rise> defines the time when a clock signal changes its value from a 0 to a 1. The statement may contain more than one <fall> and <rise> command, which defines a "multi-pulse" negative clock. The <list of signals> statement is a list of all the negative clock signals that have the above timing specifications.

OUTTIM STB=<time>
<list of signals>

The OUTTIM STB statement defines the time in ns when output signals will be strobed (compared). The <list of signals> statement is a list of all the output signals that have the same strobe time.

BUSTIM DT=<time1>STB=<time2>
<list of signals>

The BUSTIM DT statement defines the time in ns for bi-directional signals. The <time1> defines the stimulus time of the signals when they are inputs, and <time2> defines the strobe time of the signals, when they are outputs, in ns.
The <list of signals> statement is a list of all the bi-directional signals that have the same stimulus and strobe times.

For above timing, please see the tester limitations shown in Section 5.2.

3. Signal and Vector Section

This section defines the order of the signals, and lists the vector patterns. The Signal and Vector section begins with the word @SIGNAL#VECTOR /CYCLE and ends with the words #ENDVEC and @ENDSIG. The first statement in this section is the ORDER statement, which defines the order of the signals in the pattern list. This is followed by the pattern statements, which lists one line for each vector.

5.4 CTV

3. Signal and Vector Section (con't.)

The input word values may be one of the following :

0	=	Logic 0
1	=	Logic 1
Z, z	=	Tri-state
P, p	=	Positive clock pulse
N, n	=	Negative clock pulse

The output word values may be one of the following :

0, L, l	=	Logic 0
1, H, h	=	Logic 1
X, x	=	Don't care (comparison is masked)
Z, z	=	Tri-state

Input columns sequentially from left to right, insert a column space between inputs and outputs, and continue with output columns from left to right.

5.5 Example CTV File

The following is an example of the CTV format. The font is changed to Courier, which is non-proportional (equal-width characters), so that vertical columns will align properly.

```
@TIMING
     CYCLE 500
     INTIM DT=10
     'IN' 'TI' 'SHUMI' 'TIU' 'CIU' 'SHUMU' 'OEN' 'XC'
     INTIM DT=0
     'SELB' 'SELA'
     INTIM          PP = 50,200
     'CK1'
     INTIM          PP = 300,450
     'CK2'
     INTIM          PP = 100,400
     'CLOCKA'
     OUTTIM STB=490
     'SO1' 'SO2' 'SO3' 'SO4' 'SO5' 'SO6' 'OUT22'
     'OLOD' 'OPD' 'O2' 'O4' 'O8S' 'SHUMO' 'XO' 'XCN'
     BUSTIM DT=10 STB=490
     'IOL1' 'IOR1' 'IOL2' 'IOR2'
@ENDTIM
```

(signal section appears on the next page)

5.5 Example CTV File (con't.)

```
@SIGNAL
#VECTOR/CYCLE
ORDER
+    'IN' 'SELB' 'SELA' 'CK1' 'CK2' 'CLOCKA' 'TI'
+    'SHUMI' 'TIU' 'CIU' 'SHUMU' 'OEN' 'IOL1'
+    'IOR1' 'IOL2' 'IOR2' 'XC'
+    'SO1' 'SO2' 'SO3' 'SO4' 'SO5' 'SO6' 'OUT22'
+    'OLOD' 'OPD' 'O2' 'O4' 'O8S' 'SHUMO' 'IOL1'
+    'IOR1' 'IOL2' 'IOR2' 'XO' 'XCN'

$  ISSCCCTSTCSOIIIIX SSSSSSOOOOOOSIIIIXX
$  NEEKKLIHIIHEOOOOC OOOOOOULP248HOOOOOC
$   LL12O UUUUNLRLR  123456TOD  SULRLR N
$   BA  C M  M 1122         2D    M1122
$       K I  U              2     O
$       A
    000PPP000000Z0Z00 XXXXXXXXXXXXXXXXXXX   $ 1 first vector
    100PP0000000Z0Z00 XXXXXLXXXXXXXXXXXXX   $ 2
    10100P000000Z0Z00 XXXLLXXXXXXXXXXXXXX   $ 3
    00100000000Z0Z00 LLLXXXLLLLLLLLXLXLH   $ 4
    01000000000Z0Z00 LLLXXXLLLLLLLLXLXLH   $ 5
    01100000000Z0Z00 LLLXXXLLLLLLLLXLXLH   $ 6
    10000011111OZ1Z11 HHHXXXHHXHHHHHHXHXHL   $ 7
    10100011111OZ1Z11 HHHXXXHHXHHHHHHXHXHL   $ 8
    11000011111OZ1Z11 HHHXXXHHXHHHHHHXHXHL   $ 9
    11100011111OZ1Z11 HHHXXXHHXHHHHHHXHXH1   $ 10
    100PP0000000Z0Z00 XXXXXLXXXXXXXXXXXXX   $ 11
    11000011111101Z1Z1 HHHXXXHHXHHHHHXHXHHL   $ 12
    11100011111101Z1Z1 HHHXXXHHXHHHHHXHXHHL   $ 13
#ENDVEC
@ENDSIG
```

5.6 YTV Format (Chip Express print-on-change)

YTV is one of the test vector formats that is accepted by Chip Express. The YTV format consists of two files :

1. The test vectors data file
2. The control file (contains the order of the signals in each vector, and the functionality of each signal.

1. The Test Vector Data File

This file has all the test vectors in ASCII format. Each vector has two fields: the time-stamp field, and the test vector data field. The following is an example test vector file in YTV format. The font has been changed to Courier (equal width letters) so that all the columns will align.

```
  0.0ns 0011010000000111001 1XX0111111111 1XXXXXXXXXXXXXXXXXXXXXXX
  0.1ns 0011010000000111001 1XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
  0.5ns 0011010000000111001 1XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
  0.9ns 0011010000000111001 1XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
200.0ns 0011010000000111001 0XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
200.1ns 0011010000000111001 0XX0111111111 1XXXXXX1XXXXXXXXXXXXXXX
201.0ns 0011010000000111001 0XX0111111111 1XXX0XX1XXXXXXXXXXXXXXX
201.2ns 0011010000000111001 0XX0111111111 1XX00XX1XXXXXXXXXXXXXXX
201.3ns 0011010000000111001 0XX0111111111 1X000XX1XXXXXXXXXXXXXXX
201.4ns 0011010000000111001 0XX0111111111 10X00XX1XXXXXXXXXXXXXXX
201.5ns 0011010000000111001 0XX0111111111 10X0011100XXXXXXXXXXXXX
201.6ns 0011010000000111001 0XX0111111111 10X0011100XXXXXXXXXXZZZ
202.2ns 0011010000000111001 0XX0111111111 10X0011100XXXXX000X0ZZZ
500.0ns 0011010000000111001 0110111111111 10100111100XXXXX000X0ZZZ
600.0ns 0011010000000111001 1110111111111 10100111100XXXXX000X0ZZZ
600.1ns 0011010000000111001 1111111111111 10100111000XXXXX000X0ZZZ
```

The time stamp field should be in ns. The string "ns" doesn't have to appear, but if it does, there should be no spaces between the timing data and the "ns". For example, the following line is legal:

```
200.0ns 0011010000000111001 0XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
```

The following line is legal:

```
200.0   0011010000000111001 0XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
```

The following line is illegal:

```
200.0 ns 0011010000000111001 0XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
```

The following line is illegal:

```
200.0µs  0011010000000111001 0XX0111111111 1XXXXXX0XXXXXXXXXXXXXXX
```

The data field of the YTV file shouldn't have any spaces; it should be one long string.

5.6 YTV Format (con't.)

Each signal should have only one bit in the vectors. If a signal is a bi-directional, it should have another bit that is its control-enable signal. Tri-state buffers may have control signals, but they are not mandatory.

The signals can appear in ANY order.

The best way to generate the file is by generating a print-on-change simulation printout. If stimulating the inputs and strobing the outputs were done at a specific time after the beginning of each clock cycle, it would be advantageous to have the cycle time, and the timing of the different inputs and outputs, relative to the clock.

2. The Control File

The control file contains data about the functionality of the signals, and the actual order of the signals in the test vectors. The control file has a section that defines all the signals, and a section to define the strobing command. The definition of the signals must appear in the file. The strobing command is optional.

Signal Definition

This part of the file must start with BEGIN_SIGNALS, and end with END_SIGNALS. The general format of the signals definition part of the file is:

```
BEGIN_SIGNALS
signal_name signal_function [additional_data]
.
.
signal_name signal_function [additional_data]
END_SIGNALS
```

The available functions are:

1. INPUT
   This signal is a regular input. It is defined as :
   ```
   wr_n INPUT
   ```
2. OUTPUT
   This signal is a regular output. It is defined as :
   ```
   data_1 OUTPUT
   ```
3. TRI
   This signal is a tri-state signal that has a control signal in the test vector input file. Following the TRI statement comes the control-enable signal name. If the signal is a tri-state output without the control signal in the file, the right definition will be a regular OUTPUT declaration. For example, a tri-state output signal named "t_OUT_1", with a control signal named "en_222", will be defined as :
   ```
   t_OUT_1 TRI en_222
   ```

5.6 YTV Format (con't.)

4. BIDIR
   This signal is a bi-directional signal, and should appear only once in the test vectors, and should have a control-enable signal. The BIDIR statement should be followed by a control signal name. For example, a bi-directional signal named "t_BI_1", with a control-enable signal named "en_345", will be defined as :

   ```
   t_BI_1 BIDIR en_345
   ```

5. IGNORE
   This is a signal that appears in the test vector file, but should not appear in the converted CTV file. For example, this signal is defined as :

   ```
   signal_11 IGNORE
   ```

6. ENABLE
   A signal which is a control-enable of a TRI signal and/or of a BIDIR signal should be defined as ENABLE. Following this should come the logic value of the control signal that causes the controlled signal to become an active **OUTPUT**. For example, a bi-directional signal named "t_BI_1" is controlled by the signal "en_345". When the control signal is a logic "1", "t_BI_1" is an output. When the control signal is a logic "0", "t_BI_1" is an input.:

   ```
   t_BI BIDIR en_345

   en_345 ENABLE 1
   ```

   In this example, when en_345 is a "1", a tri-state or bi-directional signal controlled by en_345 will be in output mode. When en_345 is a "0", a tri-state signal will be in tri-state mode, and a bi-directional signal will be in input mode.

Strobing Commands

The strobing command is optional. There are three options to use, but only one of them can be used in each file.

1. USE_OUTPUT_AT
   This command takes an integer as a parameter. The program will use the output value only of those vectors whose timing field is a exact, even multiple of the parameter of this command. For example, if the USE_OUTPUT_AT statement is

   ```
   USE_OUTPUT_AT 200,
   ```

   and the input vectors are :

```
  0.0ns 00110100000001110011XX011111111111XXXXXXXXXXXXXXXXXXXX
  0.1ns 00110100000001110011XX011111111111XXXXXX0XXXXXXXXXXXXX
  0.9ns 00110100000001110011XX011111111111XXXXXX0XXXXXXXXXXXXX
200.0ns 00110100000001110010XX011111111111XXXXXX0XXXXXXXXXXXXX
200.1ns 00110100000001110010XX011111111111XXXXXX1XXXXXXXXXXXXX
201.0ns 00110100000001110010XX011111111111XXX0XX1XXXXXXXXXXXXX
401.2ns 00110100000001110010XX011111111111XX00XX1XXXXXXXXXXXXX
600.3ns 00110100000001110010XX011111111110X00XX1XXXXXXXXXXXXX
800.0ns 00110100000001110010XX011111111110X00XX1XXXXXXXXXXXXX
906.5ns 00110100000001110010XX011111111110X0011100XXXXXXXXXXX
1014.6ns 00110100000001110010XX011111111110X0011100XXXXXXXXXZZZ
```

5.6 YTV Format

Strobing Commands (con't.)

All the vectors will be used for the input data, but only vectors number 1, 4 and 9 will be used for expected output data.

2. STROBE_CYCLE
   This command takes an integer as a parameter. All the vectors will be used for thr input data, but only those vectors whose timing data is a exact, even multiple of the parameter, or if this does not exist, bigger than that number, will be used for expected output data. For example,

   ```
   STROBE_CYCLE 200
   ```

   If the same vectors as in the previous example are being used, then all of them will be used for input data, but only vectors 1, 4, 7, 8, 9 and 11 will be used for the expected value data.

3. STROBE_WHEN
   This command will cause the program to check the outputs only when a specific signal is changing its value. In all other cases, the outputs will be "don't care" (X). There are two options for the strobing edge :
   FALL - the strobing will be done when the signal is changing from a 1 to a 0.
   RISE - the strobing will be done when the signal is changing from a 0 to a 1.
   For example,

   ```
   STROBE_WHEN clock_in FALL
   ```

   The statement above will check the outputs of all the vectors where the value of "clock_in" is 0, and the value of this signal was 1 in the previous vector.

Radix

The default radix for all the signals is binary. You can also use a HEX radix for some or all of the signals. If you are using a HEX radix, you need to add a command after the END_SIGNALS line. This command will specify how many bits each signal should be converted to. This number can vary from 1 to 4 bits.

If the signal is binary, you should use 1.
If the signal is 2 bits HEX, you should use 2.
If the signal is 3 bits HEX, you should use 3.
If the signal is 4 bits HEX, you should use 4.

5.6 YTV Format

Radix (con't.)
In the signal declarations section, the HEX signals should be declared as different signals, and not as one bus. Please make sure to keep the right order of the signals as they are in the HEX number. For example, a 4-bit bus with the HEX value of 6 will be translated to 0100. If you define the order of the signals as :

A3
A2
A1
A0

the assignment will be : A3= 0, A2= 1, A1= 0, A0= 0.

However, If you define the order of the signals as :

A0
A1
A2
A3

then the assignment will be : A0= 0, A1= 1, A2= 0, A3= 0.

For example, assume you have the following signals :

```
a, b, c[4:0], d, e[3:2], f
```

The control file will look like this :

```
BEGIN_SIGNALS
a INPUT
b OUTPUT
c4 INPUT
c3 INPUT
c2 INPUT
c1 INPUT
c0 INPUT
d OUTPUT
e3 OUTPUT
e2 OUTPUT
f INPUT
END_SIGNALS
RADIX 1114121
STROBE_WHEN a FALL
```

Please note that the bus `c[4:0]` has 5 signals that must have 5 digits to describe them. This is why this bus was described as 14 (the first digit is a "regular" binary, and the other is a 4-bit HEX). It could be described also as 41, which means that `c4-c1` are the first HEX digit, and `c0` is the second "regular" binary digit.

5.6 YTV Format

Example of a YTV FORMAT Control File

```
BEGIN_SIGNALS
XDB7  BIDIR DBEN
XDB6  BIDIR DBEN
XDB5  BIDIR DBEN
XDB4  BIDIR DBEN
XDB3  BIDIR DBEN
XDB2  BIDIR DBEN
XDB1  BIDIR DBEN
XDB0  BIDIR DBEN
DBEN  ENABLE 0
IION  INPUT
IRWN  INPUT
OMLWN  OUTPUT
OMLRN  OUTPUT
ORSTB  OUTPUT
IAB2  INPUT
IAB1  INPUT
IAB0  INPUT
OFSYNC1  OUTPUT
OFSYNC0  OUTPUT
IOSCX  INPUT
OOSCX  OUTPUT
XED2  BIDIR DEEN
XED1  BIDIR DEEN
XED0  BIDIR DEEN
DEEN  ENABLE 1
IEA1  INPUT
IEA0  INPUT
OAO  OUTPUT
IALE  INPUT
XAD7  BIDIR ODEN
XAD6  BIDIR ODEN
XAD5  BIDIR ODEN
XAD0  BIDIR ODEN
IRDN  INPUT
TEST  OUTPUT
GR  INPUT
ODEN  ENABLE 0
END_SIGNALS
STROBE_WHEN IOSCX FALL
```

6.1 The QuICk® System Overview

(Please refer to diagram on the next page)

6.1.1 Functional Vectors

Define the functions. Determine exactly what you want done. Completely, categorically, and absolutely define the output signals, as a function of the input signals, sequentially if clocked, over time.

6.1.2 Create A Design

The designer creates a design using models described in the selected software. The user then supplies the logic simulator with the hardware description to verify the design.

The designer may create the design using all the features of the selected environment. However, in order to create a design that can be fabricated by Chip Express, the designer must use QuICk® hard macrocells at the low-level of the design. The QuICk® hard macrocells (component library) are part of every QuICk® Design Kit, and they contain the information necessary to drive the simulation of the design.

6.1.3 Package Definition

Package definition is the process by which a designer selects a package, assigns the input/ output signals to locations on the selected package, and specifies the locations of power and ground pads. The designer should specify the package information in a package definition file.

6.1.4 Prepare the Design for Submission - Logic Design File

After generating a design and simulating it, the user should prepare the design for physical layout generation, and subsequent fabrication by Chip Express. A package file and netlist file are needed to generate the layout of the design and fabricate the chip. A test vector file is needed to test the fabricated chip.

6.1.5 Netlisting

Netlisting is the process of generating a netlist file, in the format required by Chip Express, from the selected vendor description of the design. For example, when using the Synopsys interface, Chip Express requires a netlist in VLG format, which is a subset of Verilog HDL format.

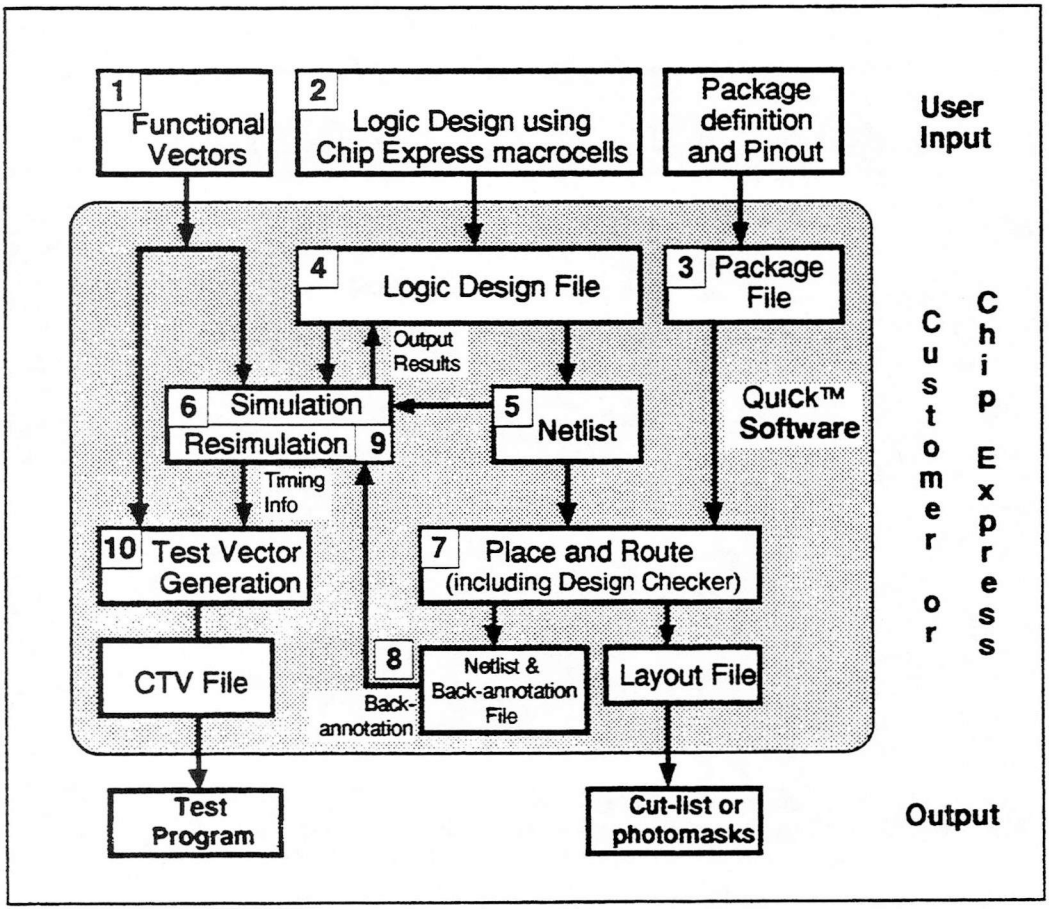
6.1.6 Simulation

The simulation step enables the user to verify the functionality and performance of the design. Simulation uses the connectivity data from the design definition, and the timing information from the component library to model the design's logical function.

The user verifies the design using the simulator. If the simulation results do not meet the requirements, the user can iterate between creating the design and simulation, until the desired results are obtained.

6.1 The QuICk® System Overview

QuICk System - Design Flow Diagram



6.1 The QuICk® System Overview (con't.)

6.1.7 Layout - Place and Route

The QuICk Place and Route software generates the layout of the design. When the physical layout of a design has been determined, a more accurate model of its signal delays can be generated. After this point, net lengths are known, and the capacitance and resistance of net routing can be calculated.

The task of the place and route program is to physically place the macro-cells on the chip, and connect all pins of the macro-cells which should be connected. The output of the place and route program is the physical representation of the design, called the layout.

The QuICk Place and Route software is fast and automatic. It was designed with the system designer in mind, and requires no chip design expertise. With it, the physical layout stage can be done by the system designer. Moving control over the physical layout to the system designer, allows significant time saving when tuning the layout to meet the performance objectives of the design, and can cut the design cycle. Chip Express uses commercially available tools for doing difficult layouts.

During the layout phase, the original netlist may be altered. One reason for this is the expansion or flattening of clock drivers, which are array dependent. Another reason may be changes that are needed in order to meet the timing specification.

In sub-micron technologies, routing delays may account for up to 70% of the total delay. Therefore, in order to reduce delays, large nets may be split into several parts. In this way, delays due to routing (RC delay) may be significantly reduced.

As a matter of clarification, all changes done to the netlist are NOT functional changes. They are changes done only to get the best performance possible.

6.1.8 Net-List and Back-Annotation

The QuICk Place and Route software also generates the back-annotation file of the design. This file contains the wire lengths of each design net. From the wire lengths, the physical capacitance of each net is calculated, and then reinserted back into the original simulation. This results in a very accurate indication of the performance of the physically-realized chip.

6.1 The QuICk® System Overview (con't.)

6.1.9 Re-simulation

Simulation with post-layout wire delays enhances the accuracy of simulation. Timing analysis with post-layout wire delays enables more accurate timing calculations. By using static timing analysis after layout, accurate design timing specifications may be produced.

6.1.10 Test Vector Generation

Test vectors are required by Chip Express in order to check the functionality of the completed chip. Test vectors should be in Chip Express's test vector format, the CTV format. Please refer to the test vector section of this manual, for detailed instructions.

Design Verification

The Place and Route software enables fast verification of the design timing and functionality after layout.

If you have QuICk Place-and-Route software on site, you can easily iterate between synthesis, simulation and layout, and optimize your designs on your own. Or if you prefer, Chip Express will perform Place and Route, and can return the back-annotation file to you.

Please Refer :

For detailed instructions on the QuICk system for VERILOG, please refer to the Verilog Design-kit Manual.

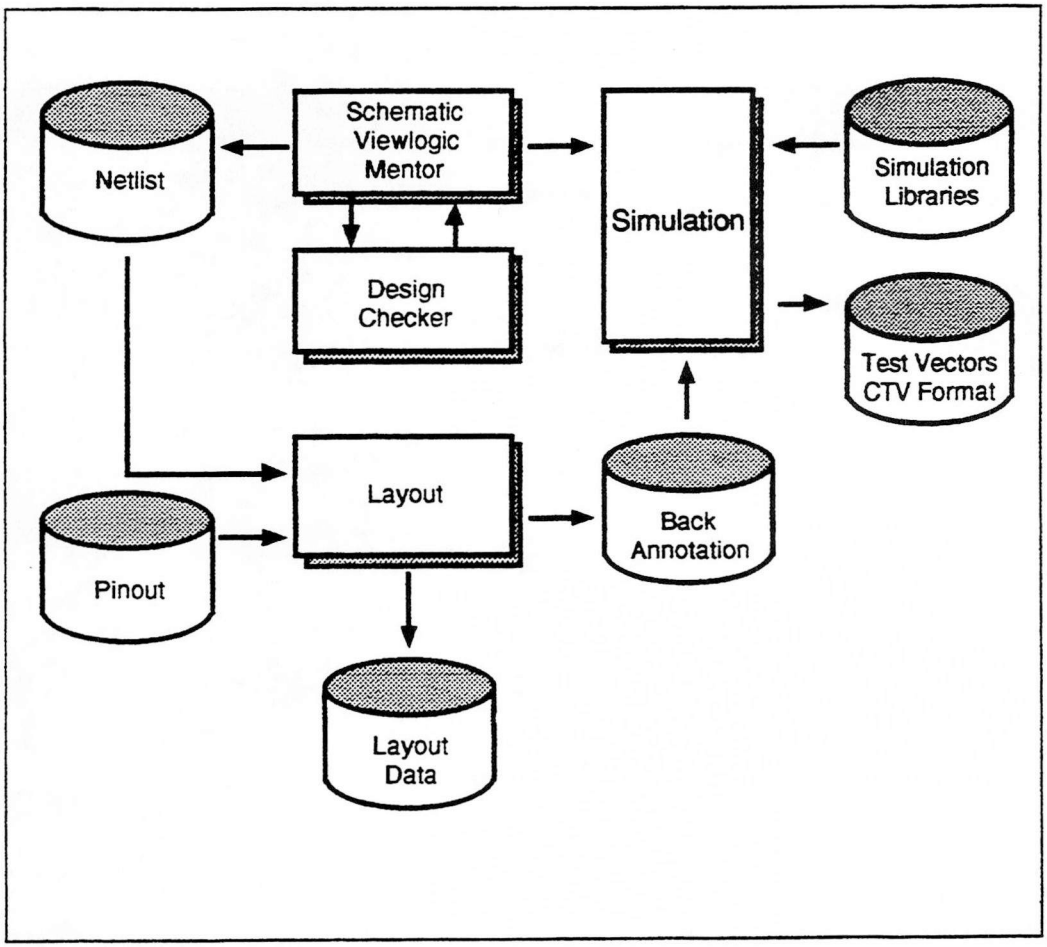
For detailed instructions on the QuICk system for SYNOPSYS, please refer to the Synopsys Design-kit Manual.

For detailed instructions on the QuICk system for VIEWLOGIC, please refer to the Viewlogic Design-kit Manual.

For detailed instructions on the QuICk system for MENTOR, please refer to the Mentor Design-kit Manual.

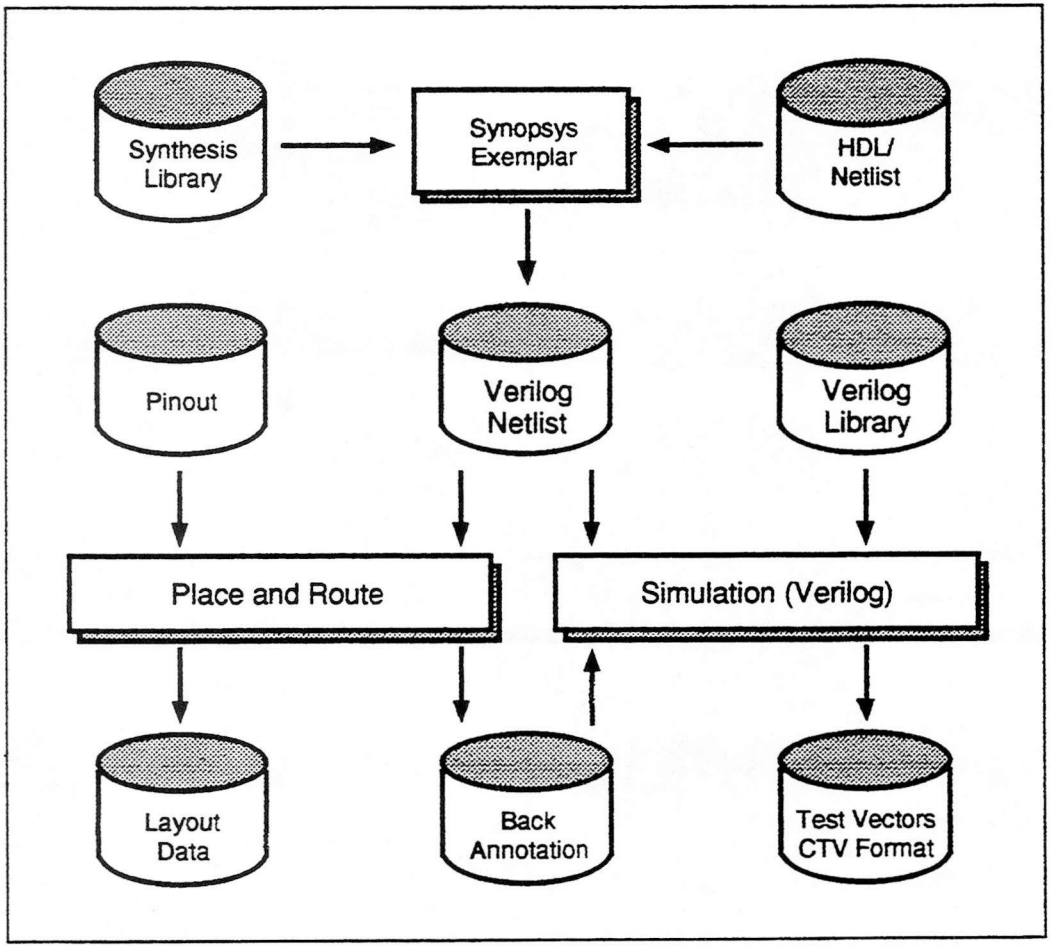
6.2 Schematic Design Flow

The diagram below illustrates the design flow when the customer uses the "schematic capture" approach.



6.3 Synthesis Design Flow

The diagram below illustrates the design flow when the customer uses the "design synthesis" approach.



6.4 Verilog Design Kit Description (Sun & HP)

Verilog Design Kit (for SUN and HP)

Verilog Design Kit Manual
Verilog Help File
Verilog Release Notes
Place & Route Software (optional)
QYH500 Macrocell Library
*Note: All design kits include relevant macrocell databooks.

QuICk Verilog Manual - Table of Contents

Overview
Process Flow
Create A Design
    Component Libraries
Simulation and Back-Annotation
    Timing Calculations
    Min./ Max. Simulation Variations
    Using the $quick_ dcalc_path Utility
    Design Verification
Test Vector Generation
    The $quick_test_gen Utility
Test Simulation
Package Definition
Netlisting
Glossary
Installation

Please Refer :
For detailed instructions on the QuICk system for Verilog, please refer to the latest QuICk Verilog Design-kit Manual, from Chip Express.

6.5 Synopsys Design Kit Description (Sun & HP)

Synopsys Design Kit (for SUN and HP)

Synopsys Design Kit Manual
Synopsys Release Notes
QYH500 Macrocell Library
Vss/VHDL QYH500 Macrocell Library
*Note: All design kits include relevant macrocell databooks.

QuICk Synopsys Manual - Table of Contents

- Overview
- Process Flow
- QuICk Libraries
  - Core Delays
- Synthesis
  - Delay Calculations
  - Operating Conditions
  - Netlisting
  - Using the ba2syn Utility
- Top Down Design
  - Design Creation
  - Layout - Back Annotation
  - Design Verification
  - Post-Layout Timing Analysis
- Glossary
- Installation

Please Refer :
For detailed instructions on the QuICk system for SYNOPSYS, please refer to the latest QuICk Synopsys Design-kit Manual, from Chip Express.

6.6 Viewlogic Design Kit Descriptions

Viewlogic Design Kit (for PC)

Viewlogic PC Design Kit Manual
Viewlogic PC Release Notes
QYH500 Macrocell Library

Viewlogic Design Kit (for SUN)

Viewlogic SUN Design Kit Manual
Viewlogic SUN Powerview Installation
Viewlogic SUN Release Notes
Place & Route Software (optional)
QYH500 Macrocell Library
*Note: All design kits include relevant macrocell library databooks.

Please Refer :
For detailed instructions on the QuICk system for Viewlogic, please refer to the latest QuICk Viewlogic Design-kit Manual.

6.7 What the Designer Sends to Chip Express :

- The netlist of the design in DDF format, or VLG format (VLG is a subset of Verilog HDL format).
- Test vectors in Chip Express format (CTV)
- A hard-copy printout of the final simulation results
- A package file that defines the selected package, number of pins, and the I/O pinout
- (optional)
  Physical layout of the design, and back-annotation file. If the user has the QuICk Place-and-Route software, he may generate the layout to be used for fabrication, and send it to Chip Express.

7.1 Introduction

At Chip Express, we know that the key to success is the customer's 100% satisfaction, based on quality, reliability, time-to-market, competitiveness, service, etc. We at Chip Express take a personal commitment to provide 100% satisfaction, using our time-to-market ASIC solution. Our solution slashes design time from months to weeks, and then provides high-volume production that is reliable, cost effective, and free from any conversion hassles.

Chip Express can deliver one-day turn-around gate arrays, using our own patented LPGA (Laser-Programmable-Gate-Array) in our microfab in Santa Clara, CA. The base wafers are made for Chip Express, at a large fabrication plant of one of our partners, such as Yamaha, TSL, etc. We use the highest quality foundries to provide world-class quality product to our customers. For example, our TSL wafer foundry is qualified by National Semiconductor, HP, IBM, Motorola, and others.

Chip Express Technology History

- Silicon Foundry for IC Production
  - — 1986 - Founded
  - — 1990 - Opened service center and headquarters in Santa Clara, CA
  - — 1991 - Introduced 1.2µ 2-layer metal CMOS LPGA 1-day gate array
  - — 1993 - Began shipping production of "One-Mask" technology for CEC Foundry: Yamaha, Japan
  - — 1994 - Introduced 0.8µ 2-layer metal CMOS LPGA up to 80K gates
  - — 1994 - Introduced and shipped 0.8µ 2 & 3-layer metal CMOS "HARD" array, low-cost, high-volume production with one-day prototyping
  - — 1995Q2 - Introducing 0.6µ 3-layer metal CMOS, LPGA & HARD array
- Current Main Customer Base
  - — AST Research, Canon, Hewlett Packard, Intel, IBM National Semiconductor, Network Peripherals, etc.
- Process Highlights
  - — ISO-9002 plan in progress
  - — World Class subcontractors (all ISO-9000 certified, or in certification process)
  - — SPC - Statistical Process Control yield monitoring
  - — Extensive qualification program
  - — Process qualification

7.2 Qualification

Chip Express emphasizes die/package reliability with suppliers who value short feedback loops on quality and reliability tests and monitors. Each new package type from a supplier will be qualified by Chip Express. When a new die in an approved assembly package from an existing device family is smaller or less complex than the qualification device, Chip Express will review construction and other immediate data, but may not require additional qualification tests. However, any larger die in the device family will be treated as a new device for qualification purposes. Any data accepted within a device family will be noted.

A device family is :

designed with the same cell library
using the same design rules,
using the same electrical rules,

fabricated on the same fab line,
using the same process flow,

assembled on the same assembly line,
using the same lead-frame composition (Eftec copper, alloy 42, etc.)
using the same die-attach eutectic and molding compound,
using the same wire composition and diameter, and

tested with the same tester model and tester frequency.

In order to maintain acceptable supplier status, the last 3 out of 3, or 4 out of 5 lot qualification series for the device family (or equivalent) should have been accepted. Data for deviations from the above will be reviewed with the Supplier Assessment Team PRIOR to release of any pre-production or production lot.

7.3 Reliability Monitors

Chip Express does not only provide a single point-in-time qualification, but it also periodically monitors the supplier's product in a series of reliability tests, to assure both Chip Express and its customers of the consistency of our product.

The following is a list of standard qualification test methods used by Chip Express to qualify our vendors. (This additional data is above-and-beyond the wafer and assembly house reliability data that follows).

	Test	Conditions	Reference Standard		LTPD/n(c)
			MIL-STD 883C	JIS C 7022 EIAJ STD	
1	High Temp. Operating	tA=125°C, Vdd=5.5V	M1005	B-1	LTPD 10% (0)
2	HAST (t=100hours)	tA=131°C, RH=85%, Vdd=5.5V		B-5	LTPD 10% (0)
3	Pressure Cooker	tA=121°C, RH=100%		IC-121-18	LTPD 10% (0)
4	Temp. Cycling	-65°C/RT/150°C (30/5/30 min)	M1010	A-4	LTPD 10% (0)
5	Thermal Shock	-65°C/150°C (5/5 min), 100 cycles	M1011	A-3	LTPD 10% (0)
6	Resist. to Solder Heat	260°C, 10 sec., or 245°C, 10 sec.		A-1	LTPD 10% (0)
7	Mark Permanence	3 parts, 4 solvents			3 (0)
8	Mechanical Dimensions	125 parts visual, plus laser scan			125 (0)
9	Solderability	230°C, 5 sec., resin flux	M2003	A-2	LTPD 10% (0)
10	ESD - Human Body	C=150pf, R=1.5KΩ, ±2000V	M3015.7	IC-121-20	5 (0)
11	Latch-up	C=500pf, R=470Ω, ±150V		JEDEC 17	5 (0)

7.4 Change Control

Chip Express works closely with its suppliers, and will notify its customers 90 days prior to the implementation of a change that will affect the form, fit or function of a Chip Express product. This definition extends to the quality and reliability programs of Chip Express suppliers.

7.5 ISO-9002

Chip Express is currently on track to achieve ISO-9002 certification in the first quarter of 1996. The ISO-9002 status of the Chip Express vendors is as follows :

Tower, Yamaha -	Foundries	- Certified
Yamaha, TSL, ASE -	Assembly and Test	- Certified
IPAC -	Assembly	- In certification (due 3Q'95)
ISE/IQL -	Final Test, Reliability Test	- Certified

7.6 Wafer Foundry Data

7.6.1 Tower Semiconductor Limited (previously National Semi. fab)

- Foundry for IC production ("HARD Array" high-volume products)
  - 1984 - Founded as National Semiconductor pilot line
  - 1993 - Tower founded (NSC/DSSI & TIC)
  - 1994 - Introduced 0.8µ 2-layer metal CMOS
  - 1995 - Introducing 0.6µ 3-layer metal CMOS
- Current main customer base
  - National Semiconductor, Hewlett Packard, Motorola
- Process Highlights
  - On-line, paperless controls and SPC measures
  - Parametric testing
  - Sample all lots at poly and metal
  - Wafer level reliability program
  - Process qualification — 3 products, 3 lots per product
- Reliability : 1.8 FIT over 2,600 parts (0.8µ process)
  0.6µ process starts qualification test in Q2'95

Product : TS80D 0.8µ 2-layer metal CMOS from T.S.L.
Test Results

Value Added Activity	Test Method	Pro-duct	Pre-con	168 Hours	500 Hours	1000 Hours	2000 Hours	Com-ments
Product Related	HTOL (infant mortality, accelerated life at 125°C)	A B		0/2601 0/231	0/2552 0/154	0/1981	0/999	
Foundry Related	HAST (85/85%)	A B	0/1170	0/1170 0/231	0/1170 0/231	0/554	0/554	
Package Related	Temperature Cycling Thermal Shock Resistance to Solder. Heat Solderability Lead Integrity Pressure Pot (ACLV) Pressure Pot - wafer level, (WL ACLV)	A A A	0/1354	 0/45 4/271	0/1083	0/783	0/600	 Passed

7.6 Wafer Foundry Data

7.6.2 Yamaha Corporation, Japan

- Foundry for IC production (LPGA and OneMask - low to medium volume)
  - 1984 - Founded
  - 1990 - Introduced 1.2µ double-metal CMOS
  - 1992 - Introduced 0.8µ double-metal CMOS
  - 1993 - Started to ship Chip Express "OneMask" parts to customers
  - 1994 - Introducing 0.65µ double-metal CMOS
- Current main customer base
  - Chip Express, Sega, Yamaha (ASSP sound products), Xilinx
- Process Highlights
  - ISO-9000 Certified
  - SPC Measures
  - Parametric testing
  - Process qualification — 3 products, 3 lots per product
- Reliability : 0.8µ OneMask device passed 2000 hour operating life (3 lots)
  0.65µ process qualified in 1994

7.6 Wafer Foundry Data

7.6.2 Yamaha Corporation (con't.)

FD-Gate Array Reliability Test Results

	Test Items / Conditions	Device= / Base Die= / Die Size= / Package= / Test #=	Device A QYH530 9.59 x 9.59mm 208-QFP R.1418	Device B QYH530 9.59 x 9.59mm 208-QFP R.1451	Device B QYH530 9.59 x 9.59mm 208-QFP R.1490	Device C QYH520 8.31 x 8.31mm 208-QFP R.1587	Device D QYH545 11.38 x 11.38mm 208-QFP R.1588
1	High Temp. Operating tA=125°C, Vdd=5.5V	168h	0/120	0/120	0/89	0/22	0/22
		500h	0/120	0/120	0/89		
		1000h	0/120	0/120	0/89		
		2000h	0/120	0/120	0/89	—	—
2	High Temp. Storage ta= 150°C	168h	0/45	0/45	0/45	0/22	0/22
		500h	0/45	0/45	0/45		
		1000h	0/45	0/45	0/45		
		2000h	0/45	0/45	0/45	—	—
3	High Temperature High Humidity Bias Ta= 85°C, RH= 85% Vdd= 5.5V	168h	0/120	0/60	0/45	0/22	0/22
		500h	0/120	0/60	0/45		
		1000h	0/120	0/60	0/45		
		2000h	0/120	0/60	0/45	—	—
4	Pressure Cooker Ta= 130°C, RH=85%	120h	0/45	0/45	0/45		
		240h	0/45	0/45	0/45		
		360h	0/45	0/45	0/45	—	—
		600h	0/45	0/45	0/45	—	—
5	Pressure Cooker (After solder heat) Ta= 130°C, RH=85%	120h	0/45	0/45	0/45		
		240h	0/45	0/45	0/45		
		360h	0/45	0/45	0/45	—	—
		600h	0/45	0/45	0/45	—	—
6	Temp. Cycling -65°C/R.T./150°C	100 cyc.	0/45	0/44	0/45	0/22	0/22
		200 cyc.	0/45	0/44	0/45		
		500 cyc.	0/45	0/44	0/45		
		700 cyc.	0/45	0/44	0/45	—	—
		1000 cyc.	0/45	0/44	0/45	—	—
7	Therm. Shock -65/150°	100 cyc.	0/45	0/45 (50cyc)	0/45		
8	Resist. to Solder Heat 245°C, 10 sec.	Tester	0/45	0/45	0/45		
		Visual	0/45	0/45	0/45		
9	Low Temp. Bias Ta= 40°C, Vdd= 5.5V	168h	0/45	0/45	—	—	—
		500h	0/45	0/45	—	—	—
		1000h	0/45	0/45	—	—	—
		2000h	0/45	0/45	—	—	—
10	Low Temp. Storage Ta= -65°C	168h	0/45	0/45	0/45	—	—
		500h	0/45	0/45	0/45	—	—
		1000h	0/45	0/45	0/45	—	—
		2000h	0/45	0/45	0/45	—	—

7.7 Assembly Plant Data

7.7.1 ASE, Taiwan

- Facility
  - — 90,000 square feet manufacturing area
  - — Options to 45,000 square feet at phase 2
  - — 16,000 square feet 10K clean room for pre-mold operations
- Assembly for high-density, surface mount semiconductor packages
  - — 1983 - Founded
  - — 1992 - ISO-9000 certified
  - — 1994 - 3,450 employees
- Current Customer Base
  - — Major worldwide customers
- Revenue
  - — 1993 - >$250M U.S.
- ASE Process
  - — Hands-off, magazine-to-magazine assembly line, featuring
    - Package reliability program
    - Very high yields, high volumes
    - Wide product availability (BGA, TQFP, etc.)

7.7 Assembly Plant Data

7.7.1 ASE, Taiwan (con't.)

ASE TQFP Package Reliability Test (Example)

Package Type	TQFP (Thin Quad Flat Pack)
Dimensions	24 x 24 x 1.4 mm
Pin Count	176 Leads
Die Size	316 x 314 mils
Pad Size	374 x 374 mils
Epoxy	Sumitomo 1076A
Lead Frame Material	Copper
Gold Wire Diameter	1.3 mils
Molding Compound	Sumitomo 7320HG
Process Flow	ASE Standard
Sample Size	45 units

ASE Test Results

	Test	Conditions	Results
1	Moisture Absorption	tA=25°C, RH=85% tA=25°C, RH=40%, RH=60%	0/45
2	Temp. Cycling	tA=-65°C to 150°C 100, 500, 1000 cycles	0/45
3	Thermal Shock	tA=-55°C to 125°C, 10, 50, 100 cycles	0/45
4	Lead Fatigue	force= 0.085 ±0.014 ounces	0/45
5	Sequential Test	T/C=10 cycles, 22 hour bake at 125°C 168 hour bake at 85°C, RH=30%	0/45
6	Solderability	245°C ±5°C, 5 sec.	0/45
7	Mark Permanence		0/45
8	PTH (PCT)	tA=121°C, pressure=15 psi, RH=100%	0/45
9	THB	tA=85°C, RH=85% (48, 96 & 168 hours)	0/45
10	Elec. Characterization	capacitance and inductance	0/45

7.7 Assembly Plant Data

7.7.2 IPAC Assembly Factory, USA

- Facility
  - — 40,000 square feet manufacturing area
  - — Options to 82,000 square feet
  - — 9,000 square feet clean room for pre-mold operations
- Assembly for high-density, surface mount semiconductor packages
  - — 1993 - Founded
  - — Jan. 1994 - Shipped production product
  - — Nov. 1994 - Introduced staggered wire bonding
- Current customer base
  - — Weitek Semiconductor, Sierra Semiconductor, others
- IPAC Process
  - — Hands-off, magazine-to-magazine assembly line, featuring
    - Kaijo FB-118B wire bonders
    - Dai-Ichi Seiko GP-ZETT multi-plunger automolds
  - — Agreement with local test facility for seamless back-end operations
  - — Package reliability program
  - — Local package engineering and technology support

IPAC Qualification and Reliability Data (1994 Summary)

	Test	Conditions		Results
1	Temp. Cycling	MIL-STD-883, Method 1010, Cond. C, E Test	100 cycles 250 cycles 500 cycles 1,000 cycles	0/386 0/443 0/134 0/125
2	Thermal Shock	MIL-STD-883, Method 1011, Cond. B, E Test	100 cycles	0/45
3	Pressure Pot	tA=121°C, pressure=15 psi, unbiased, E test (200 units pre-conditioned with 200 temp. cycles)	96 hours 96 hours	0/59 0/218
4	Mark Permanence	MIL-STD-883, M-2015		1/248
5	Heat Resistance	t=260°C, 10 seconds		0/55
6	Solderability	MIL-STD-883, M-2003, 8 hours steam age		0/129
7	Operating Life	Dynamic, 150°C, Biased, E test	168 hours 336 hours	0/135 0/135
8	Package Cracking	Per IPC - Bake, soak (C/R.H.), I.R. - 3x, C-SAM		0/74
9	Dye Penetrant	Zyglo P=Pot 60 PSIA, clean, UV / Visual, mech. decap		0/25

7.8 Chip Express HARD Array Reliability Results - 0.8µ process

CS80 0.8µ 2-layer metal CMOS from TSL, assembled by ASE and IPAC

Value Added Activity	Test Method	Product	Precon	50 Hours	100 Hours	168 Hours	500 Hours	1000 Hours	Conditions
Product Related	HTOL (infant mortality, accelerated life at 125°C)	D, D2				0/105	0/105	0/105	
	Latch-up	D	0/4	±500mA					
	Latch-up	DF	0/5	±500mA					100 pins
	Latch-up	DS	0/1	±500mA					100 pins
	ESD (Machine model)	D	0/4	>2,000V					100 pins
	ESD (Machine model)	S	0/4	>4,000V					144 pins
	ESD (Human model)	D	0/4	> 400V					144 pins
Foundry Related	HAST (131/85%)	D		0/36	0/36				100 Hrs.
	HAST (131/85%)	D2		0/45	0/45				100 Hrs.
Package Related	Temperature Cycling	D	0/45						200 cyc.
	Thermal Shock	D	0/45						100 cyc.
	Resistance to Solder. Heat	D	0/45						
	Solderability	D	0/5						
	Lead Integrity	D	0/5						
	Pressure Pot	D	1/77			1/77*			
	Pressure Pot	D2	0/60			0/60			

*Assembly related

8.1 Design Checklist

- Complete the design function description
  - — Make sure all design functions are defined (Continuing to add features can push a design up to the next die size, and delay implementation).
  - — Prepare the functional vector list; the vectors describe the exact way that the circuit must work.
  - — Make sure all required interface pins are defined.

- Logistics
  - — Determine the number of parts that you will require
  - — Select a production option, based on parts needed

- Select a software interface
  - — Chose a vendor that you are familiar with
  - — Cadence, Mentor, Synopsys, Verilog, Viewlogic, etc.
  - — If using a PC platform, select the Viewlogic option

- Select a technology
  - — For example, the QYH400 series for small size, or
  - — the QYH500 series for high-speed

- Implement the design
  - — Use Chip Express QuICk® design software.
  - — Use the Chip Express macrocell library.
  - — Calculate the power dissipation.
  - — Calculate critical path speeds.
  - — Observe the design "Do's and Don'ts"
  - — Examine testability; if a problem, include test features on the chip (BIST, est.).

Send to Chip Express :

— CTV File
Test vectors in Chip Express CTV format.

— Package File
Contains the package type, pin names, etc.

— Design File
Send the appropriate QuICk® software output, or, have Chip Express perform the QuICk® conversion for you, if you prefer the "full-service" interface.

— Simulation Output File
Show the results of the final pre-layout simulation.

8.2 Production Request Interface Sheet (page 1 of 2)

Company : _____ Application : _____ Ver._____

Chip Name : _____ Gate count : _____

LPGA Array : _____ HARD Array : _____

Package Type : _____ Bond. Diagram ID : _____

Output drive : 2mA ❑ 4mA ❑ 8mA ❑ 12mA ❑ >12mA ❑

# of outputs : ___ ___ ___ ___ ___

Vcc pins assigned : _____ Gnd. pins assigned : _____ (1 pair for each 64mA)

Testing : ❑ Standard test (functional test using the prototype part test vectors as supplied by the customer ...1MHz. functional , 25°C., 5.0V)

❑ Special Test (additional information required)

Ship to :

_____
company

_____
attention

_____
address

_____
building/ MS, etc.

_____
city state zip

Technical Information : (to be filled in by the customer & Chip Express apps. eng.)

	Standard Conditions	Other conditions
Post layout simulation :	1 ❑ Min. (60%)	4 ❑ Min.= (_____%)
	2 ❑ Typ. (100%)	
	3 ❑ Max. (170%)	5 ❑ Max.= (_____%)

Fault simulation : ❑ Fault coverage= _____% (if known)

LPGA Prototype Evaluation :

	Voltage	Temperature
1	❑ Min. (4.75V)	❑ Min. (0°C)
2	❑ Typ. (5.00V)	❑ Typ. (25°C)
3	❑ Max. (5.25V)	❑ Max. (70°C)

LPGA Process Corners :	Actual speed
❑ Best case	❑ _____MHz.
❑ Nominal case	❑ _____MHz.
❑ Worst case	❑ _____MHz.

Power Consumption Calculation : @ 1 MHz. = _____mW.
(see attached formula) @_____MHz. = _____mW. (actual speed)

8.2 Production Request Interface Sheet (page 2 of 2)

Test Requirements :

The customer sends Chip Express the following test vectors :

Date submitted : ____ - ____ - ____

Number of vectors : _____

Vectors approved by : _____
Chip Express test engineer

LPGA parts corner test results : ❑ Pass
❑ Fail

Standard production test = Functional test using the prototype part test vectors as supplied by the customer, performed at 1MHz. frequency, 25°C and 5.00V.

Special test : Requires the approval of Chip Express.

Testing : ❑ Standard test (functional test using the prototype part test vectors as supplied by the customer ...1MHz. functional , 25°C., 5.0V)

❑ Special Test (additional information required)

Packing : ❑ Plastic trays
❑ Vacuum nitrogen pack

Approved by : Customer Engineer's Name : _____

Signature : _____

Date : ____ - ____ - ____

Comments : _____

_____

_____

_____

8.3 Prototype Package Marking Spec (page 1 of 2)

		Print Size	# of Characters per Line (max.)			
			Line 1	Line 2	Line 3	Line 4
Ceramic DIP	24-DIP	6 Pt.	Chip	10	10	8
	28-DIP	6 Pt.	Express	10	10	8
	32-DIP	6 Pt.	Logo	10	10	8
	40-DIP	6 Pt.	I	10	10	8
	48-DIP	6 Pt.	V	10	10	8
	64-SDIP	6 Pt.		10	10	8
Leadless Chip Carrier (ceramic)						
	44-LCC	6 Pt.	Chip	9	9	8
	68-LCC	8 Pt.	Express	9	9	8
	84-LCC	8 Pt.	Logo	9	9	8
Quad Flat Pack (ceramic)						
	44-QFP	Not used	Chip	—	—	—
	64-QFP	6 Pt.	Express	10	10	8
	80-QFP	6 Pt.	Logo	10	10	8
	100-QFP	6 Pt.	I	10	10	8
	120-QFP	8 Pt.	V	11	11	8
	128-QFP	8 Pt.		11	11	8
	132-QFP	8 Pt.		11	11	8
	144-QFP	8 Pt.		11	11	8
	160-QFP	8 Pt.		11	11	8
	208-QFP	8 Pt.		11	11	8
	208-QFPL	8 Pt.		11	11	8
	240-QFP	8 Pt.		11	11	8
	304-QFP	8 Pt.		11	11	8
Square Quad Flat Pack (ceramic)						
	64-SQFP		Chip			
	100-SQFP	6 Pt.	Express	9	9	8
	144-SQFP	8 Pt.	Logo	9	9	8
	176-SQFP	8 Pt.	I	9	9	8
	208-SQFP	8 Pt.	V	11	11	8
Pin Grid Array (ceramic)						
	69-PGA	8 Pt.	Chip	9	9	8
	100-PGA	8 Pt.	Express	9	9	8
	132-PGA	8 Pt.	Logo	9	9	8
	144-PGA	8 Pt.	I	11	11	8
	180-PGA	8 Pt.	V	11	11	8
	208-PGA	8 Pt.		11	11	8
	224-PGA	8 Pt.		11	11	8
	256-PGA	8 Pt.		11	11	8
	299-PGA	8 Pt.		11	11	8
Ceramic Ball Grid Array						
	352-BGA		Logo			

Notes: (see next page)

8.3 Prototype Package Marking Spec (page 2 of 2)

Marking Configuration :

Line 1 is the Chip Express logo (standard).

ALL LETTERS on Lines 2-4 are MARKED IN CAPITALS.

Only 6 point and 8 point type sizes are used.

6 point is used on small packages,

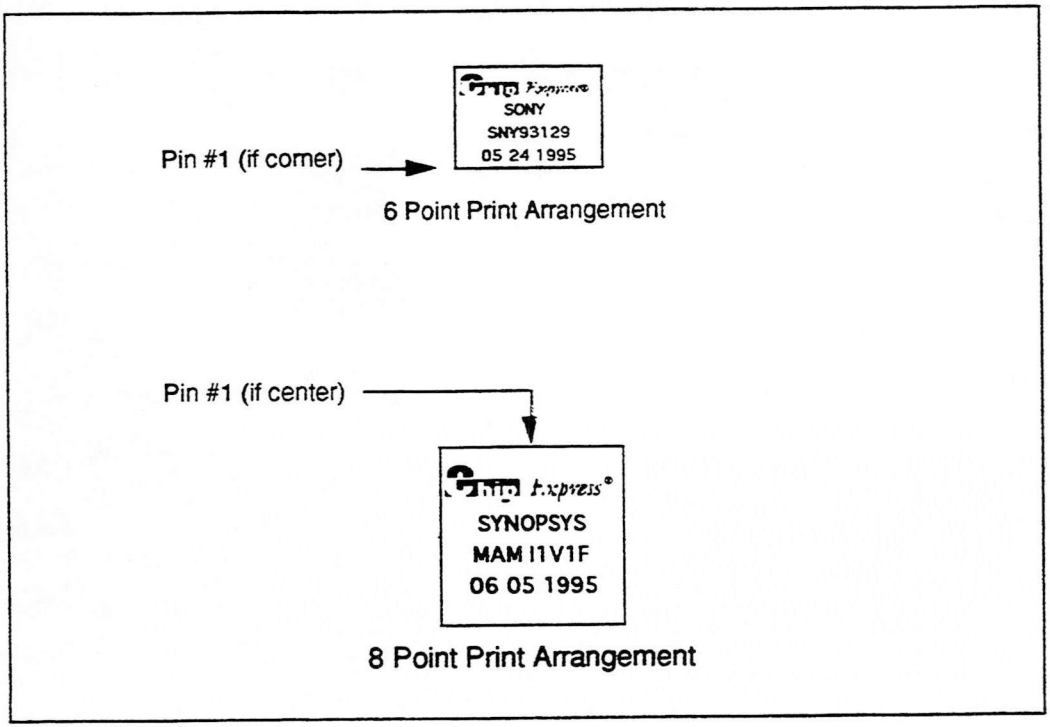
8 point is used on larger packages.

Other characters available in house are :

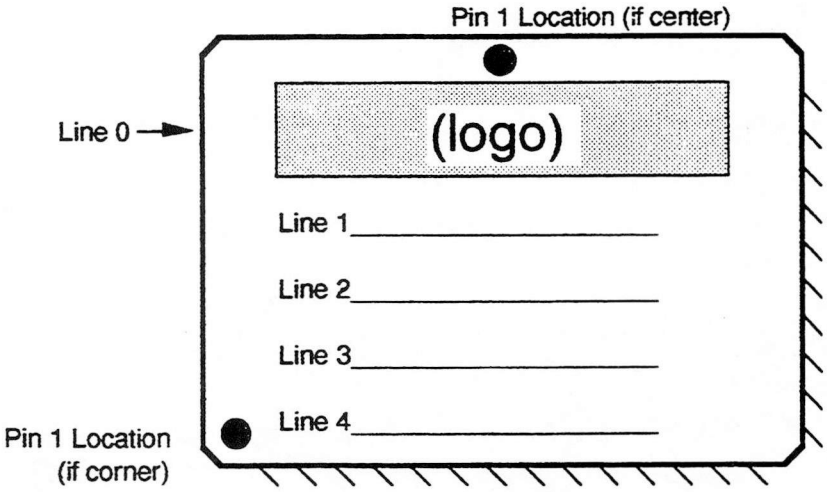
_ Underscore

- Dash

/ Backslash



8.4 Production Package Marking Spec



Line 0 : Customer's logo (default= Chip Express Logo)
Line 1 : Customer's part number
Line 2 : Customer's application name (optional)
Line 3 : Chip Express' part number
Line 4 : Seal date code, country of seal

Body Size (mm)	Character Height (pt. size)	Total # of Lines*	Number of Characters (per line)	Recommended Logo Size (max.)
10 x 10	3 point	6	8	3 x character height
14 x 14	3 point	8	10	3 x character height
14 x 20	3 point	8	13	3 x character height
20 x 20	3 point	10	13	3 x character height
24 x 24	4 point	10	13	3 x character height
28 x 28	4 point	10	13	4 x character height
32 x 32	4 point	10	13	4 x character height

* Assuming recommended logo size is used.

Approved by : Customer Engineer's Name : _____
Signature : _____
Date : ____ - ____ - ____

Manuals	# of Pages	Current Revision	Issue Date	Document Order #
QYH500 LPGA Design Manual	100pp	6-23-95	6-23-95	DB501
dQuICk® SUN Software Manual	95pp	—	1-94	Md01
QuICk® Mentor Design Manual	??pp	xx	soon	_____
QuICk® Synopsys Design Manual	65pp	—	2-93	MSY01
QuICk® Verilog Design Manual	88pp	—	1-93	MVE01
QuICk® Viewlogic PC Design Manual ..	9pp	—	6-94	MPC01
QuICk® Viewlogic SUN Design Manual..	8pp	—	5-94	MSN01
Databooks				
LPGA Package Databook	85pp	V2.1	9-94	DP01
400 Family				
QYH400 Macrocell Library Vol.1 (Gates) .	637pp	—	1-93	DL401
QYH400 Macrocell Library Vol.2 (I/Os)...	614pp	—	1-93	DL402
QYH400 Macrocell Library Summary	18pp	—	1-93	DL400
500 Family				
QYH500 Macrocell Library Vol.1 (Gates) .	391pp	—	12-93	DL501
QYH500 Macrocell Library Vol.2 (I/Os)...	587pp	—	12-93	DL502
QYH500 Macrocell Library Summary	15pp	—	2-94	DL500
Application Notes				
The QuICk® DPLL	5pp	—	7-94	AN01
Clocked RAM for QYH500	14pp	—	???	AN02
Article Reprints				
I.E.E.E. Paper	4pp	—	x-x	—

Please check with Chip Express when ordering any of the above information, since the versions are updated on a continuing basis.

Appendix A2 Design Kit Descriptions

dQuICk Design Kit (for SUN or HP)
dQuICk Design Kit Manual
dQuICk Release Notes
dQuICk Installation Notes
QYH400 or QYH500 Macrocell Library
Place & Route Software (optional)

Verilog-XL Design Kit (for SUN or HP)
Verilog Design Kit Manual
Verilog Help File
Verilog Release Notes
QYH400 or QYH500 Macrocell Library
Place & Route Software (optional)

Synopsys Design Kit (for SUN or HP)
Synopsys Design Kit Manual
Synopsys Release Notes
QYH400 or QYH500 Macrocell Library
Vss/VHDL 400 or 500 Macrocell Library
Place & Route Software (optional)

Viewlogic Design Kit (for PC)
Viewlogic PC Design Kit Manual
Viewlogic PC Release Notes
QYH400 or QYH500 Macrocell Library

Viewlogic Design Kit (for SUN)
Viewlogic SUN Design Kit Manual
Viewlogic SUN Powerview Installation Notes
Viewlogic SUN Release Notes
QYH400 or QYH500 Macrocell Library
Place & Route Software (optional)

Mentor Design Kit (for SUN or HP)
Mentor Design Kit Manual
Mentor Release Notes
Mentor Installation Notes
QYH400 or QYH500 Macrocell Library
Place & Route Software (optional)

Notes:
1. Software can be supplied on any required magnetic media.
2. All design kits include either QYH400 or QYH500 macrocell databooks.
3. List updated periodically; check with factory for latest revision.

Full Service Design Form

Business Interface Form (For full-service customers)

Date : ___ - ___ - ___

1. **Company Name** : _____
2. **Customer Contact** : _____
   Phone : (_____) _____ - _____
   FAX : (_____) _____ - _____
3. **Customer Address** : _____
   Street
   _____
   City State ZIP
4. **Business Interface Option** :

	Option 1	Option 2	Option 3
	❑ LPGA	❑ OneMask®	❑ HARD Array
Estimated # of parts to be ordered :	❑ 2 ❑ 10	❑ 10 ❑ 100 ❑ 1,000 ❑ 5,000	❑ 5,000 ❑ 20,000 ❑ 50,000 ❑ 100,000

5. **Base Array** : QYH ___ ___ ___
6. **Package** : _____ _____
   # of Pins Package Type (DIP, PGA, QFP, TQFP)
7. **Customer Interface Definition** :

Yes	No			
❑	❑	Chip Express Interface ? If not, then		Vendor
		SUN-Sparc	❑	Synopsys
			❑	Synopsys VSS
			❑	Verilog XL
			❑	Viewlogic
		PC	❑	Viewlogic
			❑	Viewlogic
		Mentor	❑	Mentor

Yes	No		
❑	❑	Other vendor netlist input format ?	Vendor : _____
_____		Gate count in this vendor's library ?	
❑	❑	FPGA design conversion required ?	Vendor : _____
		From macrocell library source _____	
❑	❑	Gate Array conversion required ?	Vendor : _____
		From macrocell library source _____	
❑	❑	Is the logic design 100% finalized ?	

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Fax: (205) 830-4058

ALASKA
Contact our Corporate
Headquarters (See California)

ARIZONA
PRO Associates
2121 W. University Dr. #124-2
Tempe, AZ 85281
Tel: (602) 921-5500
Fax: (602) 921-5468

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Southern States Marketing
1702 North Collins, Suite 250
Richardson, TX 75080
Tel: (214) 238-7500
Fax: (214) 231-7662

CALIFORNIA
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CORPORATE HEADQUARTERS
2323 Owen Street
Santa Clara, CA 95054
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Fax: (408) 988-2449

Nexus Corporation
1616 N. Shoreline Blvd.Suite A
Mountain View, CA 94043
Tel: (415) 943-1350
Fax: (415) 943-1356

PRO Associates
95 Argonaut, Suite 240
Aliso Viejo, CA 92656
Tel: (714) 588-2700
Fax: (714) 588-2710

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1500 West Canal Court, Bldg. A
Littleton, CO 80120
Tel: (303) 795-3600
Fax: (303) 795-0373

CONNECTICUT
Contact Chip Express
Eastern Sales Office
28 Silver Hollow
N. Brunswick, NJ 08902
Tel: (908) 940-1900
Fax: (908) 940-0698

DELAWARE
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Eastern Sales Office
28 Silver Hollow
N. Brunswick, NJ 08902
Tel: (908) 940-1900
Fax: (908) 940-0698

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Chesapeake Technology Inc.
3905 National Drive, Suite 425
Burtonsville, MD 20866
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Fax: (301) 384-9596

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ElectroCraft Corporate Office
2240 Belleair Rd, Suite 285
Clearwater, FL 34624
Tel: (813) 530-3788
Fax: (813) 530-9252

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9127 Chianti Ct.
Boynton Beach, FL 33437
Tel: (407) 364-0933
Fax: (407) 364-0935

Orlando
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Apopka, FL 32712
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Fax: (407) 880-7590

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Fax: (407) 694-1583

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ELCOM
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Fax: (770) 447-8340

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Headquarters (See California)

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Tel: (303) 795-3600
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2950 Metro Drive
Bloomington, MN 55425
Tel: (612) 851-7909
Fax: (612) 851-7907

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Indian Creek Office Building
10540 Marty, Suite 200
Overland Park, KS 66212
Tel: (913) 385-0390
Fax: (913) 268-9977

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Tel: (214) 238-7500
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Tel: (603) 898-6333
Fax: (603) 898-6895

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Suite 145K
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Tel: (205) 830-4001
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Fax: (603) 898-6895

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Tel: (201) 288-7400
Fax: (201) 288-7583

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Rochester, NY 14624
Tel: (716) 426-0806
Fax: (716) 268-9977

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232-Boulevard
Hasbrouck Heights, NJ 07604
Tel: (201) 288-7400
Fax: (201) 288-7583

NORTH CAROLINA
ELCOM
3060-C Business Park Dr.
Norcross, GA 30071
Tel: (770) 447-8200
Fax: (770) 447-8340

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2950 Metro Drive
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Tel: (612) 851-7909
Fax: (612) 851-7907

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Suite 210
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Tel: (513) 436-1222
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Fax: (610) 272-2866

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Suite 104
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Salem, NH 03079
Tel: (603) 898-6333
Fax: (603) 898-6895

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ELCOM
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Norcross, GA 30071
Tel: (770) 447-8200
Fax: (770) 447-8340

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Bloomington, MN 55425
Tel: (612) 851-7909
Fax: (612) 851-7907

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Huntsville, AL 35805
Tel: (205) 830-4001
Fax: (205) 830-4058

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Southern States Marketing
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Richardson, TX 75080
Tel: (214) 238-7500
Fax: (214) 231-7662

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Lange Sales
772 East 3300 South , Ste. 205
Salt Lake City, UT 84106
Tel: (801) 487-0843
Fax: (801) 484-5408

VERMONT
ITI
182 Main Street
Salem, NH 03079
Tel: (603) 898-6333
Fax: (603) 898-6895

VIRGINIA
Chesapeake Technology Inc.
14808 Fothergil Court
Burtonsville, MD 20866
Tel: (301) 236-0530
Fax: (301) 384-9596

WASHINGTON
Westmark
1800 112th Avenue NE
Suite 250E
Bellevue, WA 98004
Tel: (206) 454-1944
Fax: (206) 454-2483

WEST VIRGINIA
Chesapeake Technology Inc.
14808 Fothergil Ct.
Burtonsville, MD 20866
Tel: (301) 236-0530
Fax: (301) 384-9596

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Victory Sales, Inc.
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Suite 208
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Tel: (414) 789-5770
Fax: (414) 789-5760

For area codes 715, 608 contact:
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2950 Metro Drive
Bloomington, MN 55425
Tel: (612) 851-7909
Fax: (612) 851-7907

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Fax: 905-670-1743
Mr. Dan Heath, Vice President

CANADA (Western)

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Beijing 100086 CHINA
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Fax: 86-10-6253-6649
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e-mail: jasonsun@public3.bta.net.cn

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Nanjing 210005 CHINA
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Fax: 86-25-4201-297
Mr. Stone Chen, Managing Director
e-mail: stone@public1.ptt.js.cm

CHINA / HONG KONG

DRAGON TECHNOLOGY CO., LTD.
903 Kowloon Centre, 29 Ashley Road
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Tel: 852-2303-0711
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2323 Owen Street
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Tel: (408) 988-2445
Fax: (408) 988-2449
http://www.chipexpress.com

INDIA
Josh Bellin
CHIP EXPRESS CORPORATION
2323 Owen Street
Santa Clara, CA 95054 USA
Tel: 408-235-7376
Fax: 408-988-0513
e-mail: joshb@chipx.com

ISRAEL
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Fax: 81-44-812-6276

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DASKO CO., LTD.
23F, Korea World Trade Center
159-1 Samsung-dong, Kangnam-ku
Seoul, 135-729 KOREA
Tel: 82-2-551-3144
Fax: 82-2-551-6411
Mr. Geun-Soo Kim, Sr. Applications Engineer
e-mail: gskim@nextel.net

LATIN AMERICA & MEXICO
Josh Bellin
CHIP EXPRESS CORPORATION
2323 Owen Street
Santa Clara, CA 95054 USA
Tel: 408-235-7376
Fax: 408-988-0513
e-mail: joshb@chipx.com

SINGAPORE, MALAYSIA, & THAILAND
MAXMEGA ELECTRONICS PTE. LTD.
63 Hillview Ave. #08-12
Lam Soon Ind. Building 2366 SINGAPORE
Tel: 65-769-1118
Fax: 65-769-2221
Ms. Nicole Ho, Sales Engineer
e-mail: maxsales@singnet.com.sg

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